PET ENGINEERING COLLEGE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

UNIT – IV

INTERCONNECT,MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS

CLASS : S5 ECE

SUBJECT CODE : EC3552

SUBJECT NAME : VLSI AND CHIP DESIGN

REGULATION : 2021

NEED FOR TESTING

→ Test falls into three main categories.

① Logic verification / Functionality tests

* These are used to verify the functionality of the circuit.
* This verifies that the chip performs its intended function.
* It is used to prove that, the circuit is functionally equivalent to some specification. This specification may be VHDL, Verilog description (or) Truth table etc.

② Silicon debug

* This second tests are run on the first batch of chips that return from fabrication.
* This confirms that the chip operates as it was intended and help debug the discrepancies.
* Requires creative detective work to locate the cause of failures.

③ Manufacturing Test

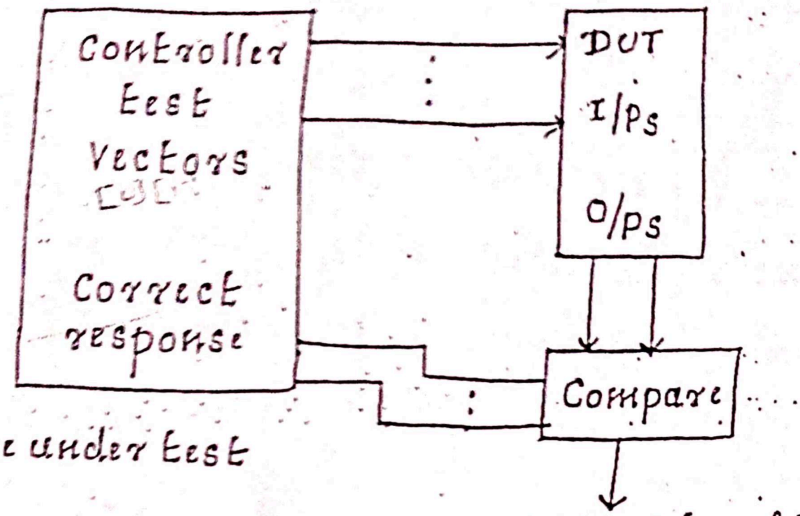
* Verify that every transistor, gate and storage element in the chip works correctly.

i) Fault: Small imperfections due to starting material or photomasking is fault.

→ Testing a chip can occur at..

	Cost of detecting malfunctio
* Wafer level	$ 0.01 - 0.1
* packaged chip level	$ 0.1 - $1
* board level	$1 - $10
* System Level	$10 - $100
* field Level	$100 - $1000

→ Overview of testing process



DUT → Device under test

* Test vector is an array of binary inputs. These are applied to DUT.
* The output is given to compare block. The actual output will be issued by controller to the compare block.
* The compare block, compares the actual o/p with the output from DUT.
* Functionality of chip is tested by this process. If any mismatch occur, it will be displayed for our reference.
* Test program is written in the controller for adder, register etc. In this program, clock cycle, clock speed, format of test data (NRZ, RZ etc) are specified.
* By using simulator, the testing can be done. The waveforms (or) Logical values (0 or 1) are applied to the simulator.
* Program is written using VHDL, Verilog etc. The o/p of the simulator is stored in the file is known as activity file. These o/p's are compared and checked.

→ Schooming process:

In this process, V_{DD} is varied from 5 to 6 volts (If $V_{DD} = 5V$), while varying the tester cycle time. The graph is drawn for measuring speed sensitivity of the part with respect to voltage.

TESTERS, TEST FIXTURES AND TEST PROGRAMS

Tester: A tester is a device that can apply a sequence of stimuli to a chip or system under test and monitor or/and record the results of those operation.

→ Test fixtures:

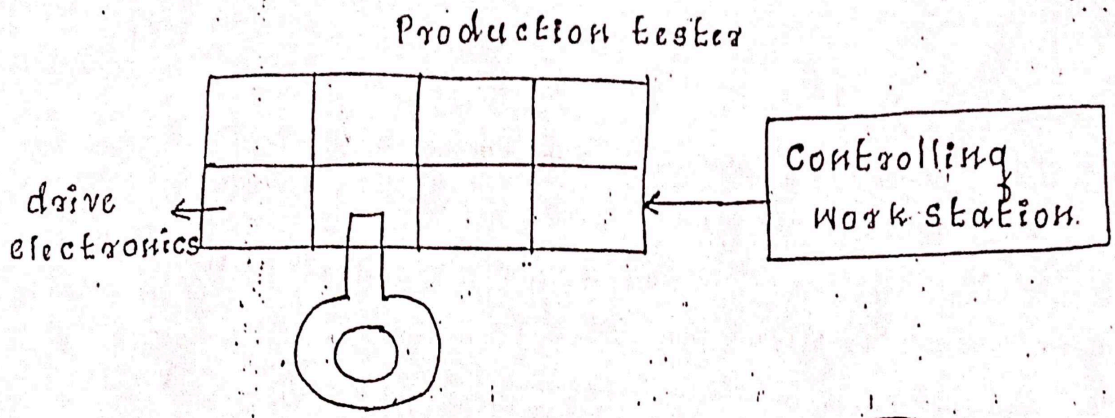
* The requirements for testing a chip is known as test fixtures. Test fixtures are,
  i) A probe card to test at the wafer level or unpackaged die level with a chip tester.
  ii) A load board to test the package with a chip tester.
  iii) A printed circuit board for bench level testing (with or without a tester)
  iv) PCB with the chip used to demonstrates the application for which the chip is used.

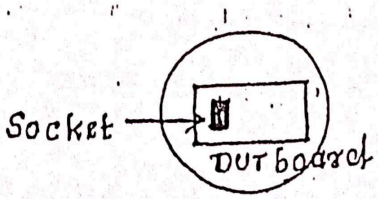
General purpose production testers :—

features:

* expensive
* Configurable I/O ports
* huge RAM for each tester pin.

* The tester drives the i/o pins from the memory on a cycle by cycle basis.





Test load board in test head.

Production tester consists of,

* four bay cabinet holding the drive electronics
* Controlling work station.
* Test head, which has probe card and load board.

* probe card or load board is connected to the tester.
* The test program is compiled, downloaded into the tester.
* The tester samples the test output and compares the values with the predefined program output.
* If there is a difference, that is marked as a faulty chip and stored for future analysis.

Probe card testing → the card is raised, moved to the next die on the wafer, lowered and test procedure repeated.

Load board testing → [the test part is removed from the board and sorted into a good or bad bin. A new part is fed to the load board and the test is repeated.]

Test programs :-

Tester requires a test program

* High level Language
* Specifies a set of input pattern and output assertion

Attributes to be setup for testers are:

* Set the supply voltage
* Assign mapping between stimulus file signal names and physical tester pins.
* Set the pins on the tester to be inputs or outputs.
* Set the clock on the tester.
* set the input pattern and output assertion timing.

On a chip basis,

* Apply supply voltage
* Apply digital stimulus and record responses
* Check responses against assertion
* Report and log errors.

→VCD (Vector change descriptions)

* These are used to compact stimulation results)

Simple stimulus pattern for full adder is,

Sl.No	a	b	c	Expected o/p
0	0	0	0	00
1	0	0	1	10
2	0	1	0	10
3	0	1	1	01
4	1	0	0	10
5	1	0	1	01
6	1	1	0	01

* Each row is known as test vector
* First column is known as test vector number.
* a, b, c are the binary values of i/p.

Clock generation :-

① The clock signal consist of clock low and clock high signals.

② The timing generator can be used. Here the clock rising edge is placed anywhere in the tester cycle.

③ Data formats – NRZ (non return to zero)
RZ (Return to zero)
SBZ (surrounded by zero)

Handlers :-

* Handler is used for feeding IC to a test fixture which is attached to a tester.
* It has mechanical positioning equipment. The status is indicated at the top that whether the handler is functioning or not.
* It can handle 2-4 chips at a time.

LOGIC VERIFICATION PRINCIPLES

① Test benches and harnesses

* Test bench or harness is nothing but HDL code. In the test bench inputs are applied to the system and outputs are taken and compared with the output of the another model.
* The model which is designed using high level language or MATLAB is known as golden model.

* Golden model writes the expected output file.
simulators can provide breaking points for the purpose of debugging.

(2) Regression Testing :-
- It is a large test bench, requires high level Language for testing.
- It automatically verifies that no functionality has changed in a module or set of module.
- It has to be done every day to check that bug fixes or feature enhancement have not broken the completed modules.

(3) Version Controlling :-
* Combining with regression testing, this is used for orderly management of different design iterations.

(4) Bug Tracking :-
* Enter the bug and bug location.
* Note the severity
e.g. of bug tracking system. UNIX | Linux

SILICON DEBUG PRINCIPLES

* First, the specific signals can be brought to the top of the chip. These are small squares of top level metal. These are known as probe points.
* The overglass cut mask should specify a hole in the passivation over the probe pads. It is used for the metal for reliable contact. These points are key points in a high speed signal chain.

* The square which is exposed can be connected with the probprobe by using microscope.
* The die can be probed electrically or optically or mechanically.
* LVP (Laser voltage probing) and PICA (picosecond imaging circuit Analysis) can be used for probing.
* silicon is partially transparent to infrared light. So LVP and PICA can be used by using the substrate.

→ To examine hotspot
* Infrared imaging can be used to examine hotspot

→ To identify temperature problems
* Liquid crystal material can be painted to a die to identify the temperature related problems.

→ FIB (Focused Ion Beam)
* If the fault Locations are identified, the FIB can be used to cut wires or lay new conductors down

→ Debugging Logic circuits
* SPICE stimulation is used for debugging Logic circuits.

Types of Failures

- Manufacturing (It occurs when a chip has a defect)
- Functional (These are physical design errors)
- Electrical (It occur if the chip is Logically Correct, but malfunction occur due to temperature voltage)

- shmoo plots:-

* In this plot, voltage is taken in the x axis and speed is taken in the y axis. The test vectors are applied and output is recorded.

MANUFACTURING TEST

- To test a combinational circuit with N inputs, need of 2^N test vectors.
- To test a sequential circuit with addition M registers need of 2^{N+M} test vectors.

→ Methods to test the circuit

① Fault model :

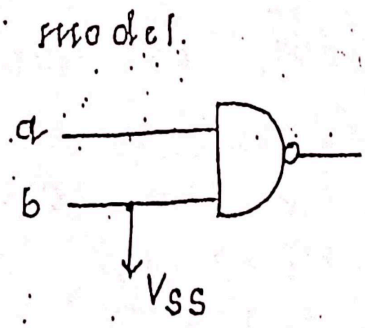
* It is the model for how fault occurs, and because of the fault what is the impact occur in the circuit.

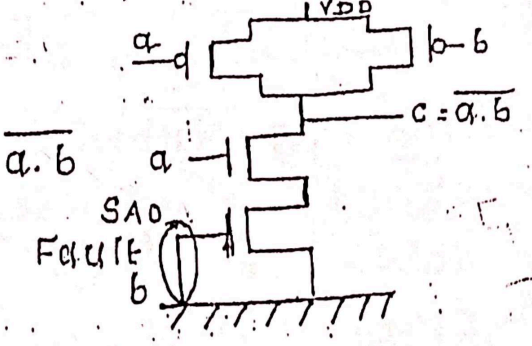
a) Stuck-at-Faults :

* Stuck-at-0 and stuck-at-1 are the fault models.

→ Stuck-At-0 Fault :

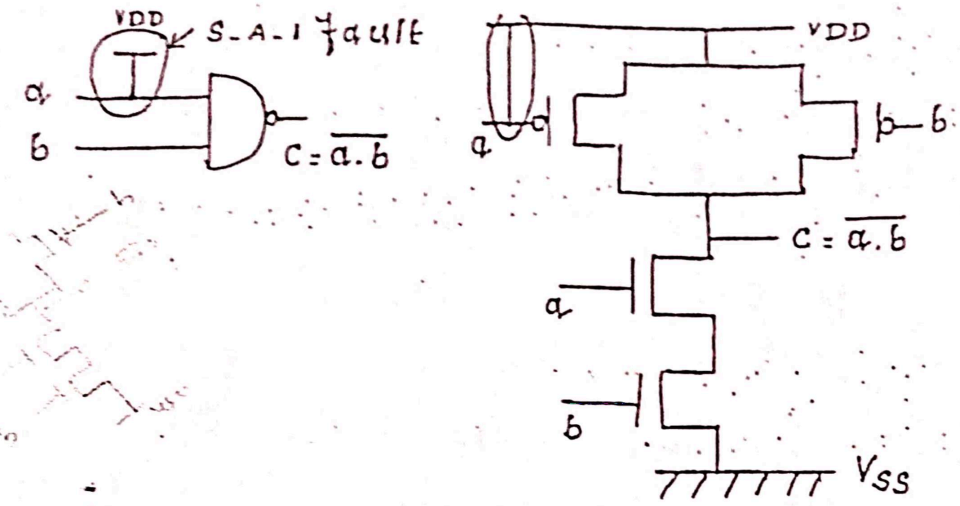
* This is due to the thin-oxide shorts. For e.g when n transistor gate is connected to Vss, fault occur in the circuit. It is modeled as Stuck-At-0 model (or) S-A-0 (or) SA0 model.





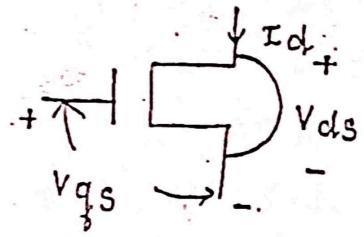
→ Stuck-At-1 Fault :

* p transistor gate is connected to V_{DD}, Fault is occured. This is known as Stuck-At-1 (or) SA1 (or) S.A1 model.

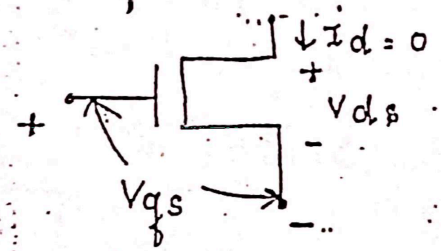


b) SC and OC Faults

*(A short circuited FET is one which always conducts drain-soure current with an applied drain-source voltage Vds) The gate has no control over the operation. (It is also known as <u>stuck-on-fault</u>)



*(An open circuit fault is exactly opposite to short-circuit fault. Open-circuit fault is known as <u>stuck-off fault</u>) In this model, current never flows regardless of Vgs (or) Vds



(2) Observability :-

* The observability of a particular node is the degree to which you can observe that nodes at the outputs of the integrated circuits.

To check the circuit operation, all the nodes should be easily observable at the output.
This results in circuit complexity and lack of design methodology.

(3) Controllability :-
* controllability of an internal circuit node within a chip is a measure of ease of setting the node to a 1 or 0 state.
* A node with little controllability will take several cycles to get it to right state.
It is impossible to generate test sequence for those circuits.
Making all flipflops resettable via a global reset signal is one step forward to good controllability.

(4) Fault coverage :-
* measure of goodness of test vector is fault coverage.
* For a single test vector; how many percentage of fault can be checked.
* Each node is set at SA0/SA1 and i/p sequence is given and the output is verified with the predefined value from a good machine.

% Fault coverage = Total no. of nodes in which fault identified / Total No. of nodes

(5) ATPG (Automatic test pattern Generation)
* If we want to test the gate which is embedded in Large logic circuit, use the existing circuit to create a specific path from the location of gate which is going to be checked for finding fault. This technique is known as path sensitization. This process of creating the path is known as propagation.

⑥ Fault Grading and Fault simulation :-

→ Grading :-

step 1 : The node to be faulted is selected (usually clock, reset nodes are avoided)

step 2 : * Each node to be faulted is set to 0 and then set to 1.

* Then test vector is applied. This result is compared with good circuit response.

* If the test vector result is not matched, with a good one, the fault is detected. Then simulation is stopped.

* The same process is repeated for finding the fault in the next node.

No. of simulation cycle $\boxed{S_k = NK}$

Where, N → Average no. of test vectors

k → no. of nodes to be faulted.

→ Fault simulation :-

Parallel simulation

* By using this simulation, we can test the more circuits.

$$S_k = \frac{KN}{\text{No. of circuits should be simulated in parallel}}$$

Concurrent simulation

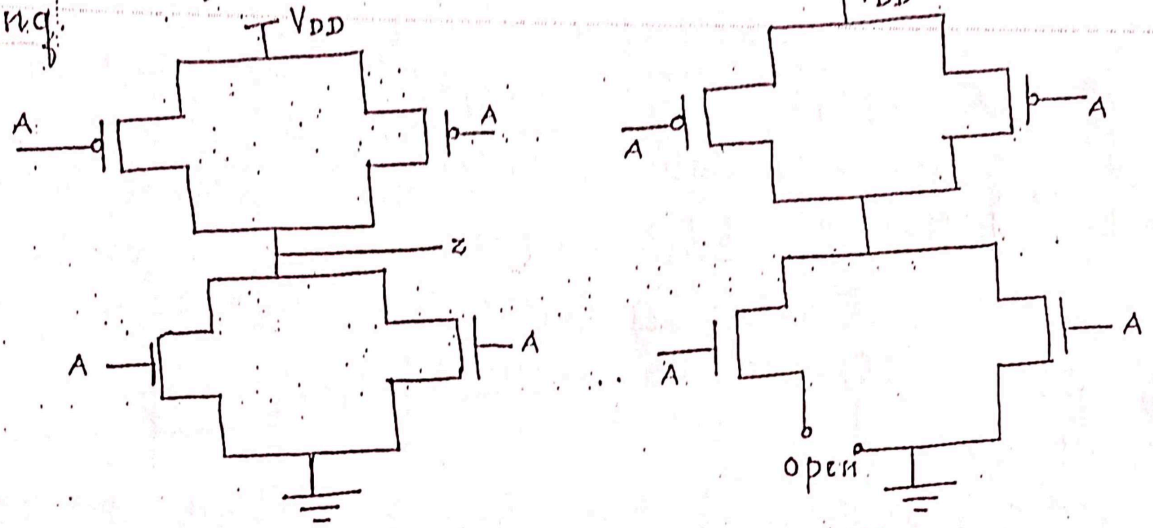
* It is a software based fault simulator.

* First the good machine (circuit) is chosen. Then faulting machine is simulated parallely with good machine.

* If there is any difference occurs between them. Then faulty machine is dropped from the queue. It means fault is detected.

(f) Delay Fault testing :-

* Failures that occur in CMOS could leave the functionality of the circuit untouched, but affect the timing.



* If an open circuit arise in the nMOS transistor source connection to ground, then the gate would still function but with increased t...

(g) statistical Fault Analysis

* It is also known as STAFAN. It estimates the probability of detection of Faults.

Statistics used for STAFAN

(a) zero counter → In each gate input, when Logic 1 to Logic 0 change occurs, then zero counter is incremented.

(b) One counter → When logic 0 to logic 1 change, then one counter is incremented.

(c) Sensitization counter → If the change in i/p causes the sensitization o/p, then, this counter is incremented.

d) Loop Counter → it detect and deals with the feedback.

* One controllability (C_1) of line $C_1(l) = \text{one.count}/N$

* zero controllability (C_0) of line $C_0(l) = \text{zero.count}/N$

* Sensitization probability $S(l) = \text{Sensitizationcount}/N$

$N \rightarrow$ No. of test vectors

* probability of detection of SA1 fault:

$$D_1(l) = B_0(l) \cdot C_0(l)$$

$B_0(l) \rightarrow$ zero observability

* Probability of detection of SA0 fault:

$$D_0(l) = B_1(l)\, C_1(l)$$

$B_1(l) \rightarrow$ one observability

⑨ Fault Sampling

* It is used in some of the circuits only. In some of the circuits, occurence of fault is not possible.

* In this circuit, nodes are randomly selected and faulted. fault-detection rate is calculated statistically

* This method will not give the specific level of fault coverage. No. of samples may be increased to get good result.

DESIGN FOR TESTABILITY

Approaches:

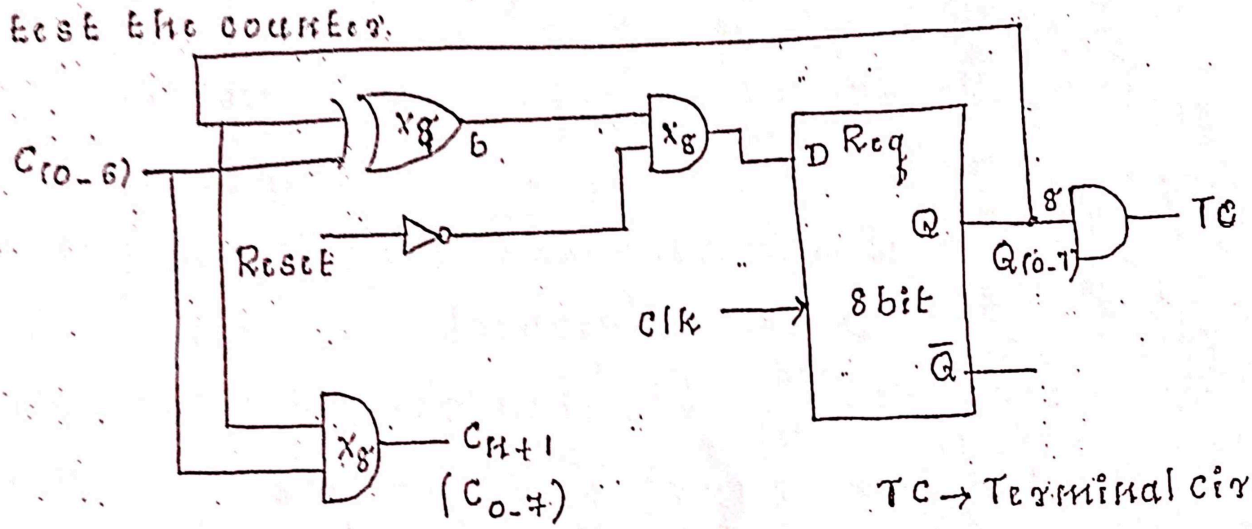
- → Adhoc testing technique
- → scan based approach
- → self testing and built-in-testing technique.

The application of these techniques are,

- → Random Logic (Multilevel standard)
- → Regular Logic array (data paths)
- → Memories (ROM, RAM)

① Adhoc testing technique:-

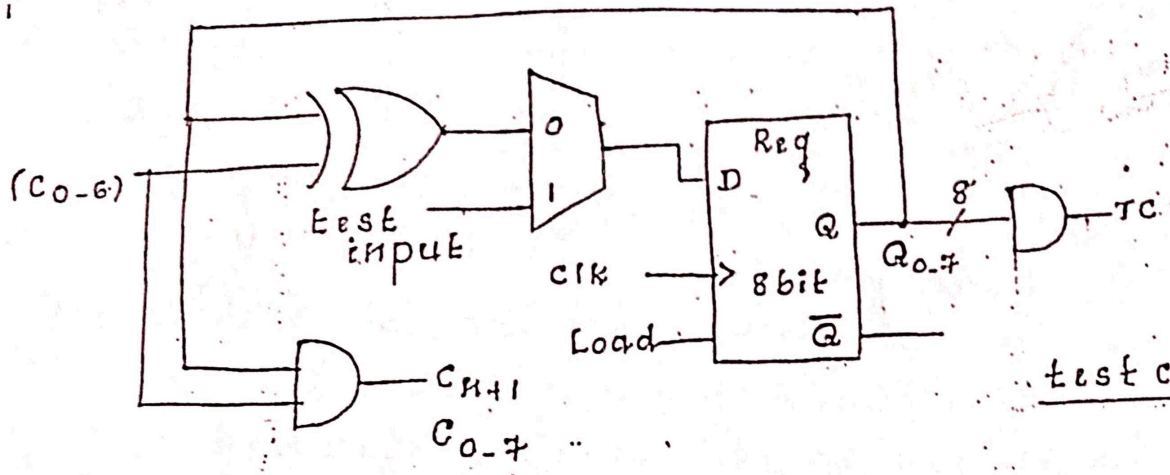
* Consider 8 bit simple counter and the techniques to test the counter.



TC → Terminal circuit

a) Testing the counter circuit:- Reset, clk signals input.

* Counter circuit can be tested for its carry propagatio
* Testing circuit will be done inside the counter.
* In this, test input signal is added as i/p to the MUX. o/p of the MUX is connected with D input.
* Load is the signal introduced in the counter circuit.
* (It enables the counter to be preloaded with some values to check for carry.)



test circuit

b) Testing the counter circuit by dividing the Long counter:-

* partioning the counter into various sub-counters will be very effective in reducing testing complexity.

e.g: To test the 16 bit counter, $2^{16} = 65536$ pulses

using dividing approach, divide 16 bit counter

↓

2, 8 bit counter

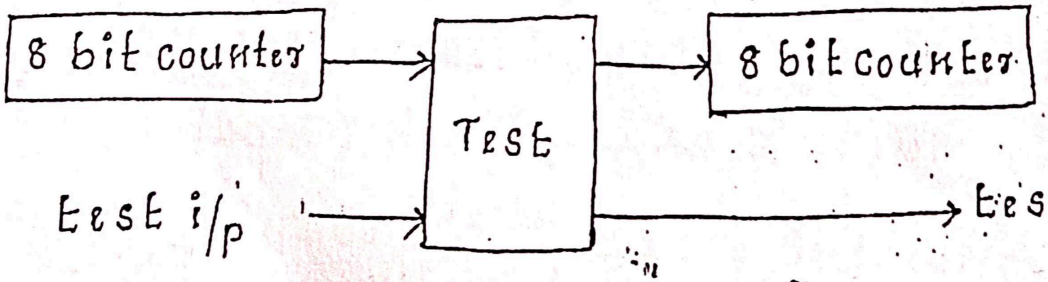
Now we want, $2 \times 2^8 = 512$ pulses only. So pulses are reduced.

testing time = 2^{16} x testing period

testing time = 2×2^8 x testing period

16 bit counter

testing time = 2^{16} x testing period

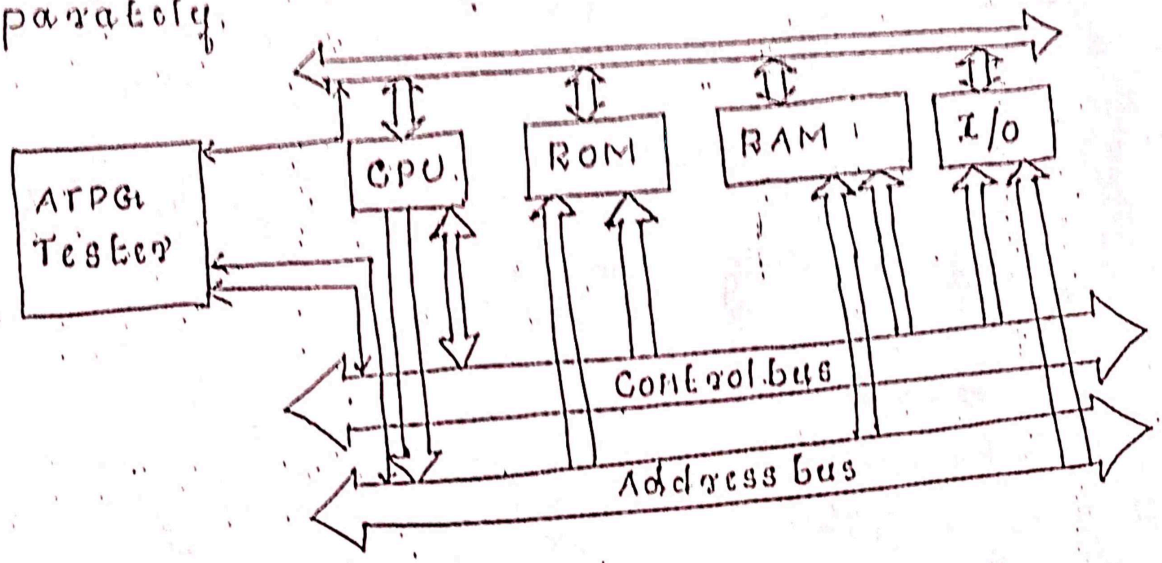


testing time = 2×2^8 x testing period

Dividing Counter approach

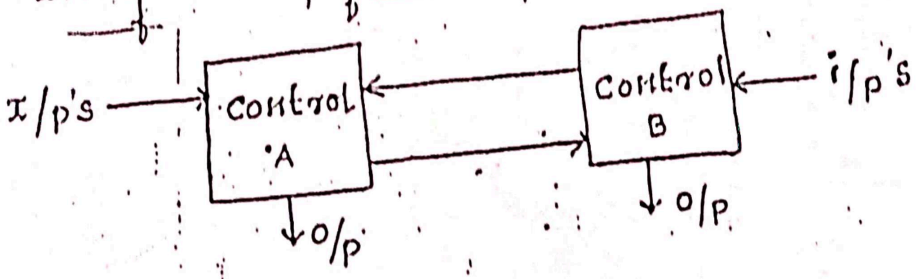
(c) Bus oriented Testing :-

* Used to test the circuit like microprocessor.
* Tester can access all the functional units which are connected by the buses. Tester can disconnect any functional unit from the bus by setting its output into high independance state.
* Test pattern for each subsystems can be applied separately.

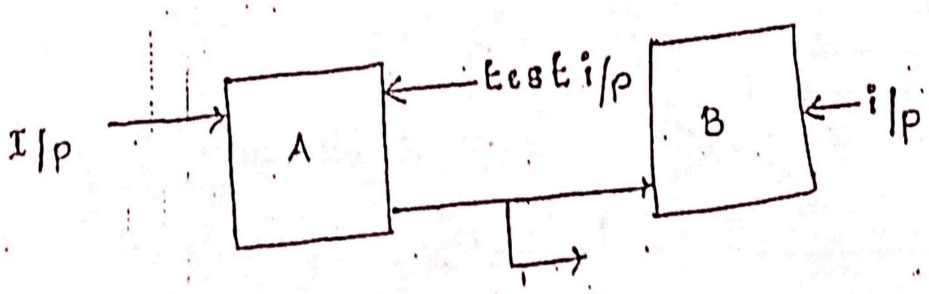


(d) Mux Based Testing :-

* This technique uses Muxes for testing. Addition of demuxes increase the observability.
* If TG muxes (Transmission gate Muxes) are used, Then they occupy less space with increase in speed.



Two modules connected normally



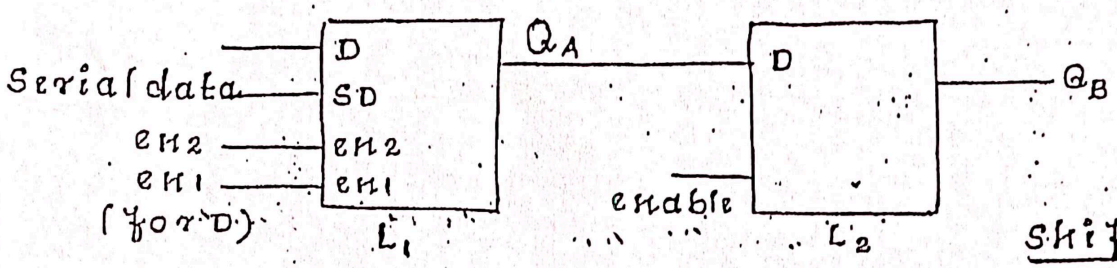
Connection to Test module A

② Scan based approaches

→ Level sensitive Scan design approach (LSSD)

* SRL - is shift register. This is the basic block for LSSD.

*(In LSSD, when input change occurs, the response is independent of the component) and wiring delays within network.



Shift Register Latch (SRL)

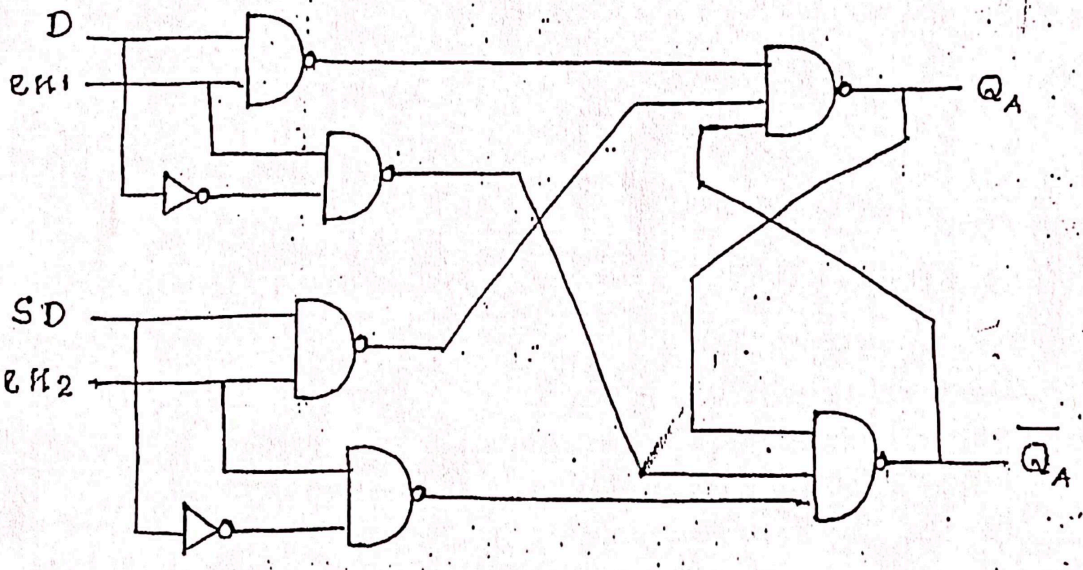
Where, en_2 → enable pin for SD

D → Data

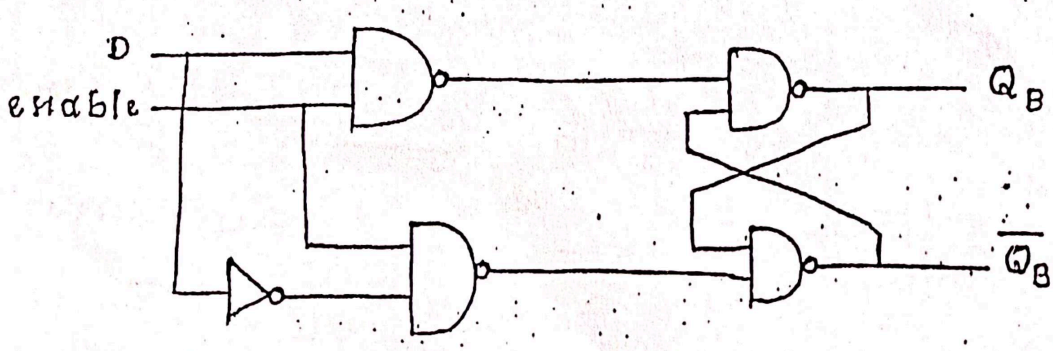
SD → Serial data

L_1, L_2 → Latches

en_1 → enable pin for D input



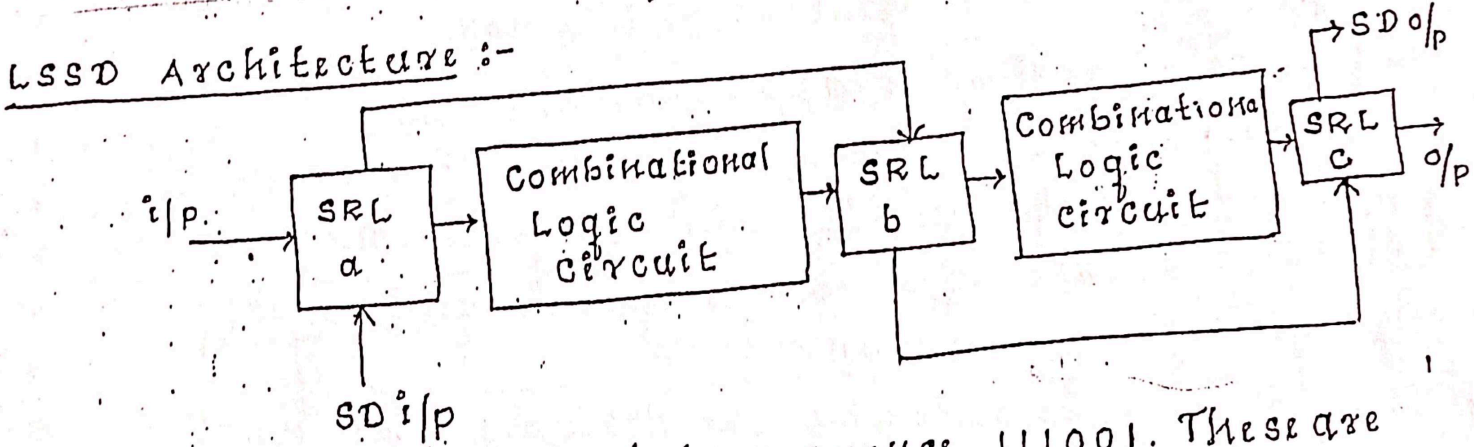
Structure of L_1



Structure of L_2

* Two Latches are connected to form SRL.
When en_1 (for D) is high, Then Q_A is set by D input.
When en_2 is high, Then Q_A is set by serial data input.
* In normal operation en_1 is enabled.
If SRL connected in series, then Q_B (of L_2) is connected with SD (of L_1).
* In L_2, if enable pin is high, then Q_B is set by D input.

LSSD Architecture :-

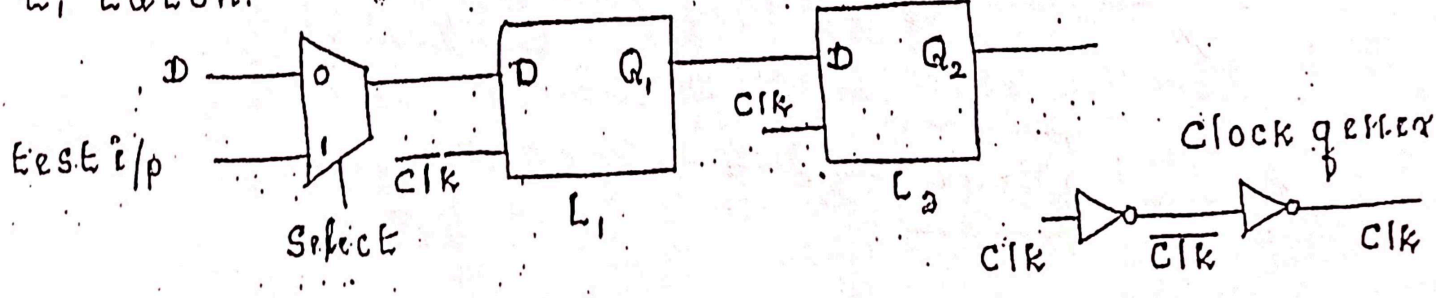


e.g To transmit the data sequence 111001. These are known as SD input. These bits are given to SD pin one by one.

* Initially 1st bit is given to SD of SRL (a)1. This bit is shifted to Qa1 o/p. Then Qa1 is connected with SD of SRL a(2). Then Qa2 is connected to SD of SRL a(3).
* After 3 clock pulses, this bit is shifted to Qa3
* The same processes happened in SRL(b). The serial data will be obtained through Q_{b1} serially.

→ Serial scan approach :-

* Similar to LSSD technique. A mux is added before L_1 Latch.

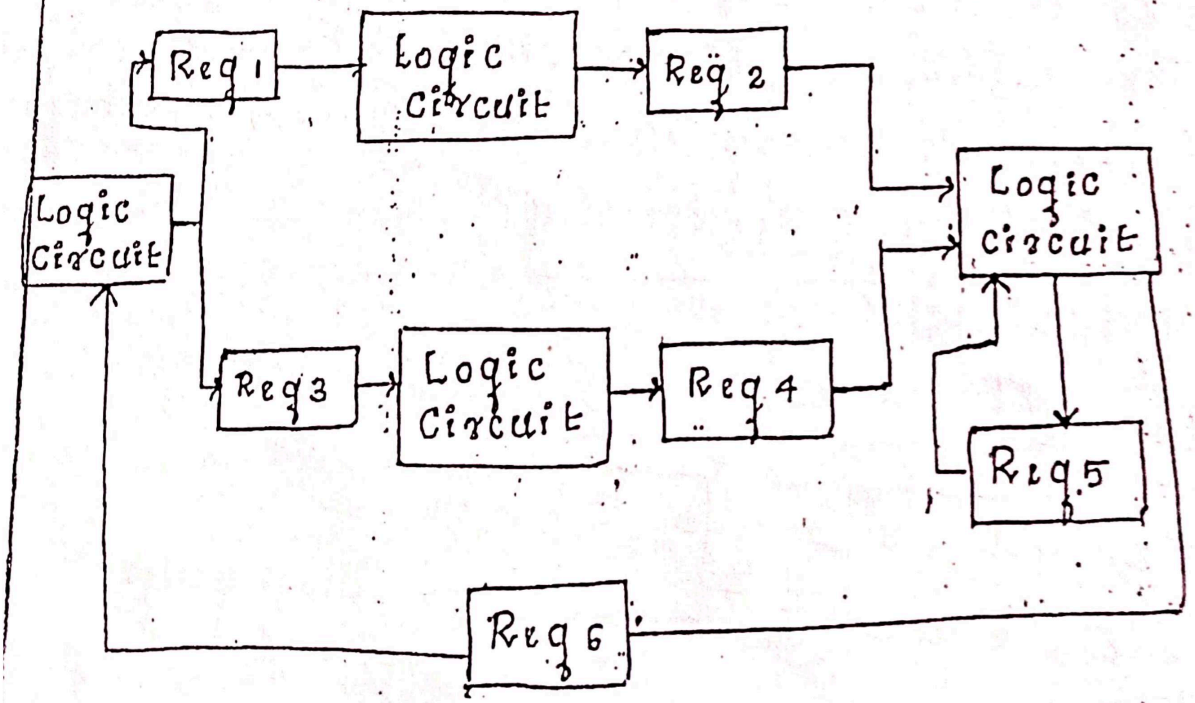


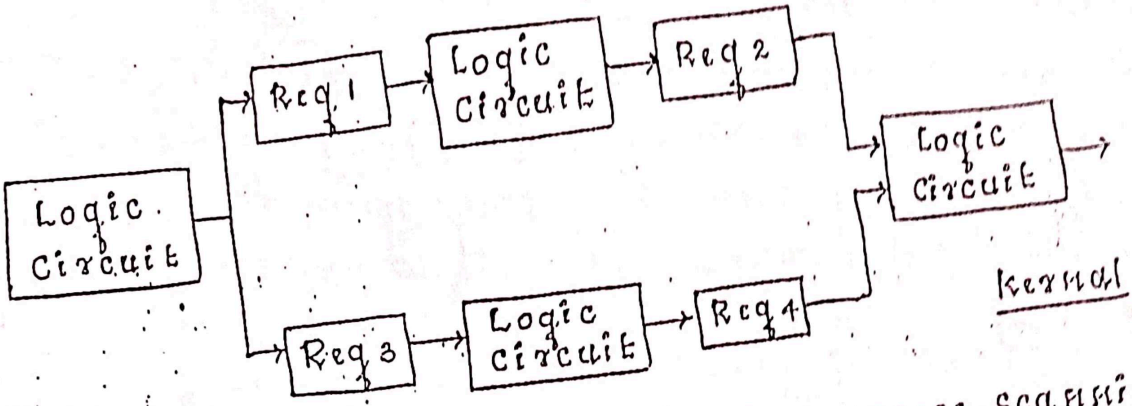
* Test input is given to the i/p of the MUX.
* When select signal is high, test input is given to D of Latch-1.
* If clk is activated, then we will get Q_1 output. Then clk is activated, the Q_1 o/p is given to the input D of Latch 2.
* Final o/p is obtained at Q_2.
* When testing is not processed. Then select is active low. Then normal operation will be done.

⟹ Partial Serial Scan approach:-

* In this approach, scanning area is increased. The test generator decides which register should be scanned. So instead of scanning all registers, only selected register are scanned.
* The decision is taken by the designer that, what are the registers should be scanned.

e.g. The tester decided that Reg 5 and Reg 6 are to be scanned, then these registers will hold their state. Except Reg 5 and Reg 6, the remaining part of the circuit to be tested is known as kernal.

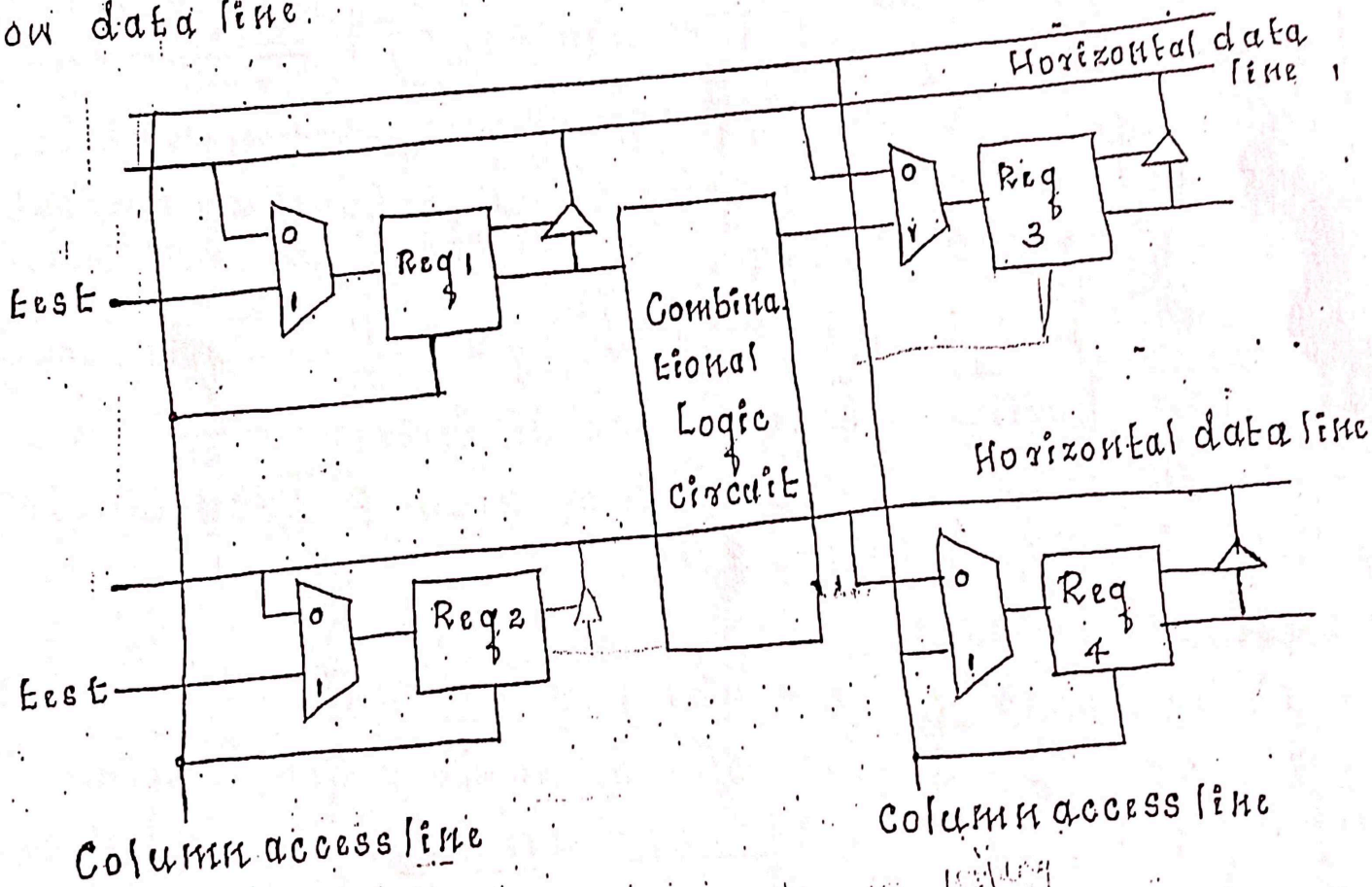




Kernal

⟹ Parallel scan Approach :- (Random access scanning)

* Consider two by two register section. Each register receives a column and row access signal along with a row data line.



(3) Self test techniques :-

Objective

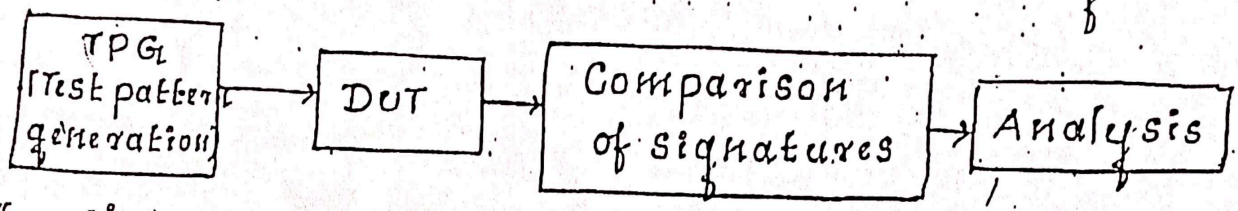
* To reduce the test-vectors generation cost
* To reduce the volume of test data.
* To reduce testing time.

→ Signature Analysis

* It performs polynomial division. polynomial division is the division of the o/p data of DUT (device under test)
* This o/p data is represented as polynomial P(x), characteristic polynomial is C(x). signature is given by,

$$R(x) = \frac{P(x)}{C(x)}$$

* This polynomial division can be done using LFSR.



* The signature from the DUT is compared with the expected signature. If these two signatures are matched, there is no fault in DUT.
* Nature of fault is identified by using analysis block.

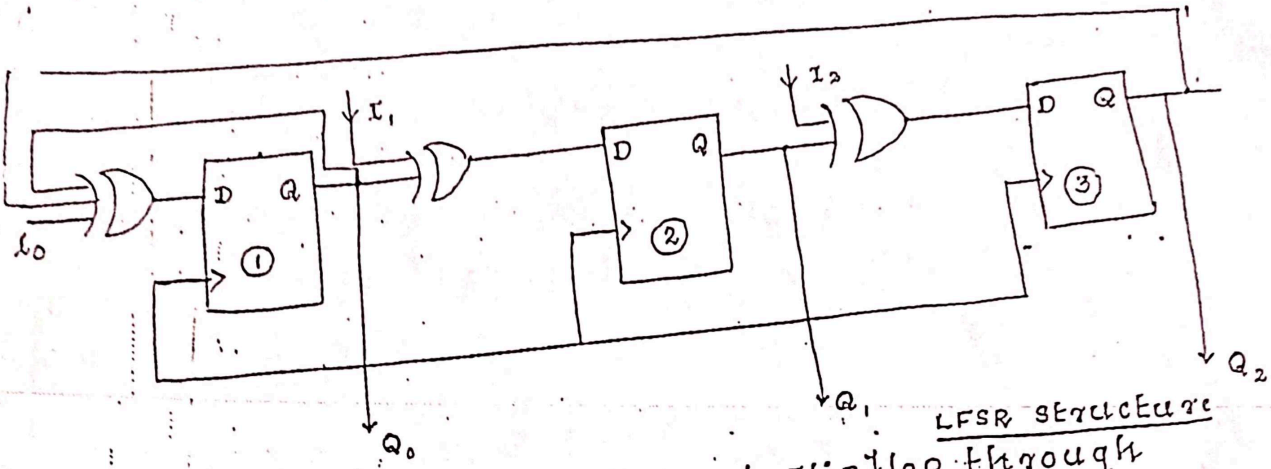
→ BILBO (Built-In Logic Block Observer):-

* The important component of BILBO is LFSR (Linear feedback shift Register).

LFSR structure:

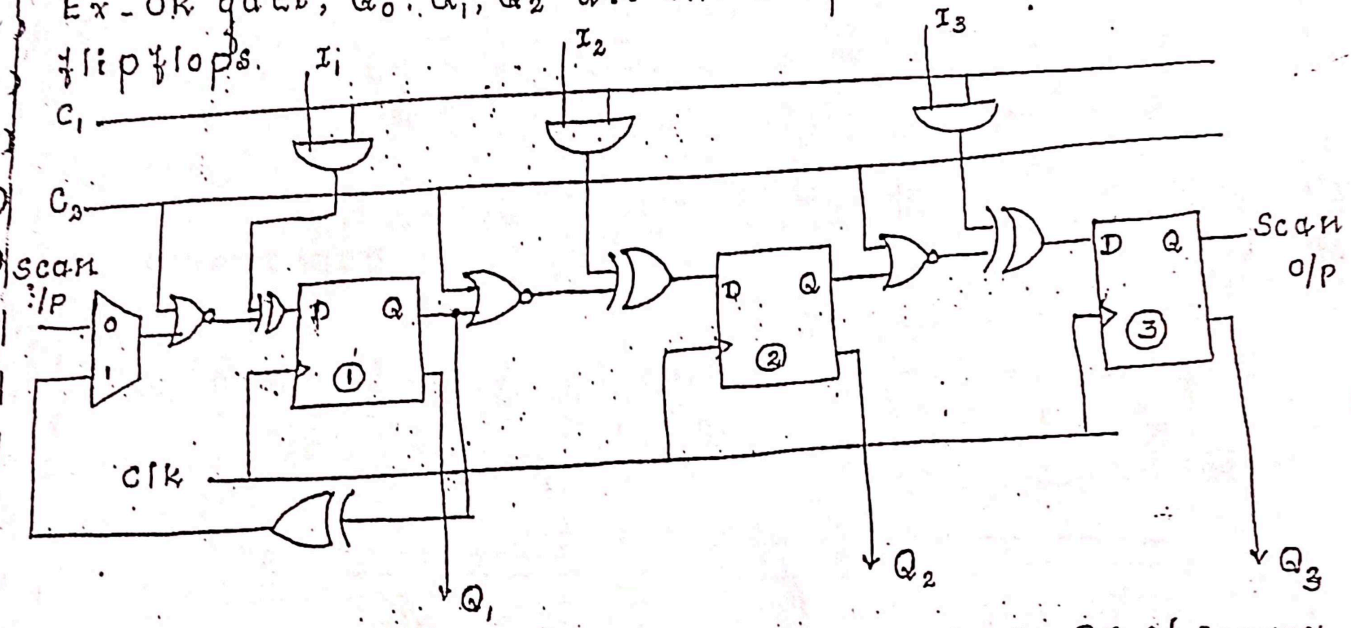
* It has storage elements and XOR gate.
* It can be used for random number generation. polynomial division in signature analysis concept.
* LFSR can be connected in series or in parallel depends upon the application.

Serial LFSR	Parallel LFSR
Size is small	Large
Speed is low	high



LFSR structure

* I_0, I_1, I_2 are inputs given to D of flipflop through Ex-OR gate, Q_0, Q_1, Q_2 are the outputs taken from three flipflops.



BILBO observer

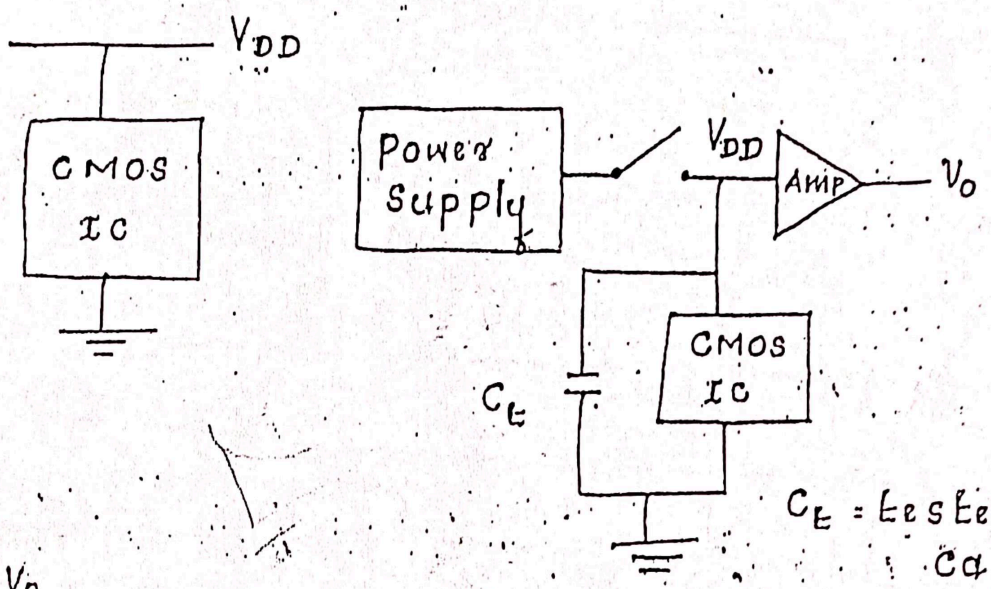
* BILBO observer has LFSR with some addition of gates can be used. C_1, C_2 are used to define certain mode.

Modes of operation:

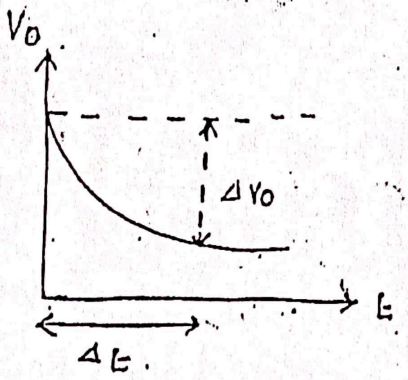
C_1	C_2	Mode
0	0	Scan mode
0	1	Reset mode
1	0	LFSR mode (Signature analysis (or) Pseudo random seq. generat
1	1	Normal mode

➡ I_{DDQ} Testing :-

* When the power supply is applied to IC, then I_{DD} current will flow.
* When the signal inputs are not switching, then quiescent leakage current I_{DDQ} can be measured.



C_t = tester capacitance



Current I_{DD} flows through CMOS IC,

$$I_{DD} = C\left(\frac{\Delta V_o}{\Delta t}\right)$$

$$C = C_t + C_{chip}$$

➡ Self Testing of Memory :-

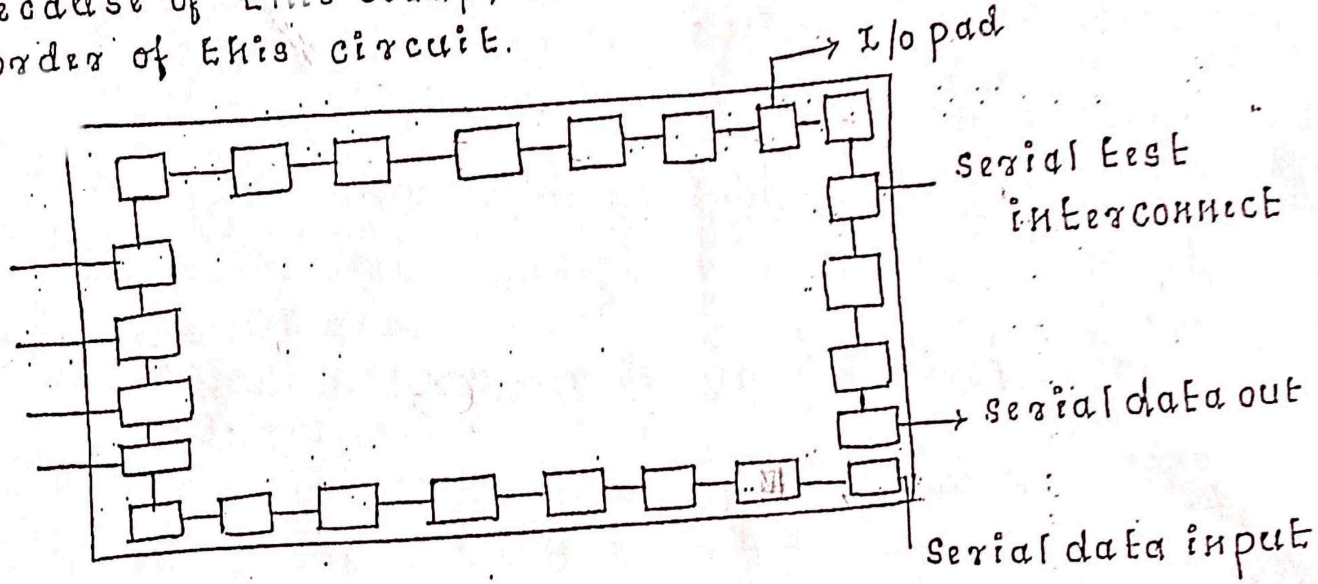
* ROM can be tested by placing signature analyzers at the output of ROM.
* After that, test mode is initiated and contents of memory of checked.
* For testing RAM memory, separate read/write memory test program was written) and RAM can be tested as ROM testing process.

BOUNDARY SCAN

Programs are used to test the complete board. Because of the complexity of the board, designers use the unified scan based test technique to test the ICs at the board. This is known as system level testing. also known as boundary scanning technique (or) boundry scan

Boundary Scan Test Architecture:- BST architecture

* BST core : of placing a shift register cell adjacent to each component pin. and to interconnect the cells.
* Because of this setup, some chain is formed around the border of this circuit.



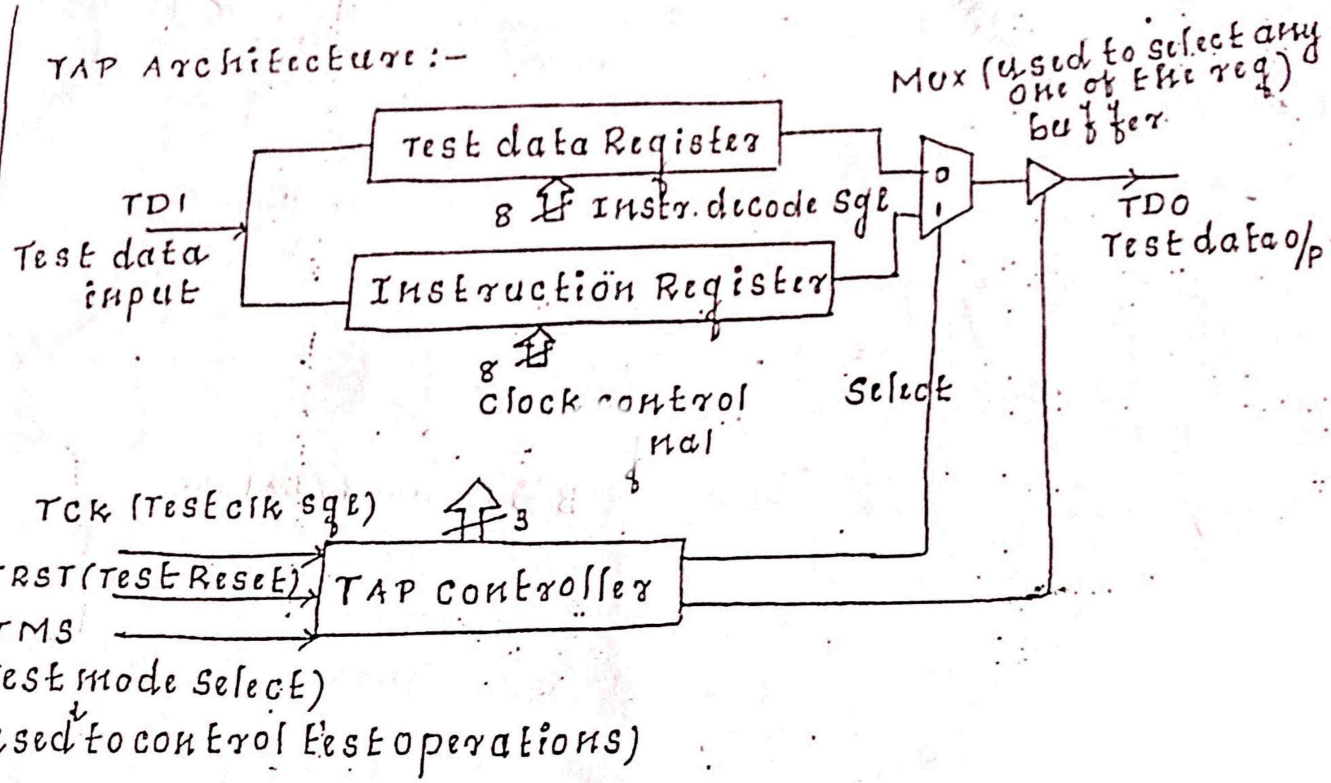
Various testing can be conducted using BST.

1. Connectivity tests between components
2. Sampling and setting i/p of an IC
3. Distribution and collection of self test results.

→ TAP (Test Access port)

* It is included in the BST Architecture.

TAP Architecture :-



* IE consists of,

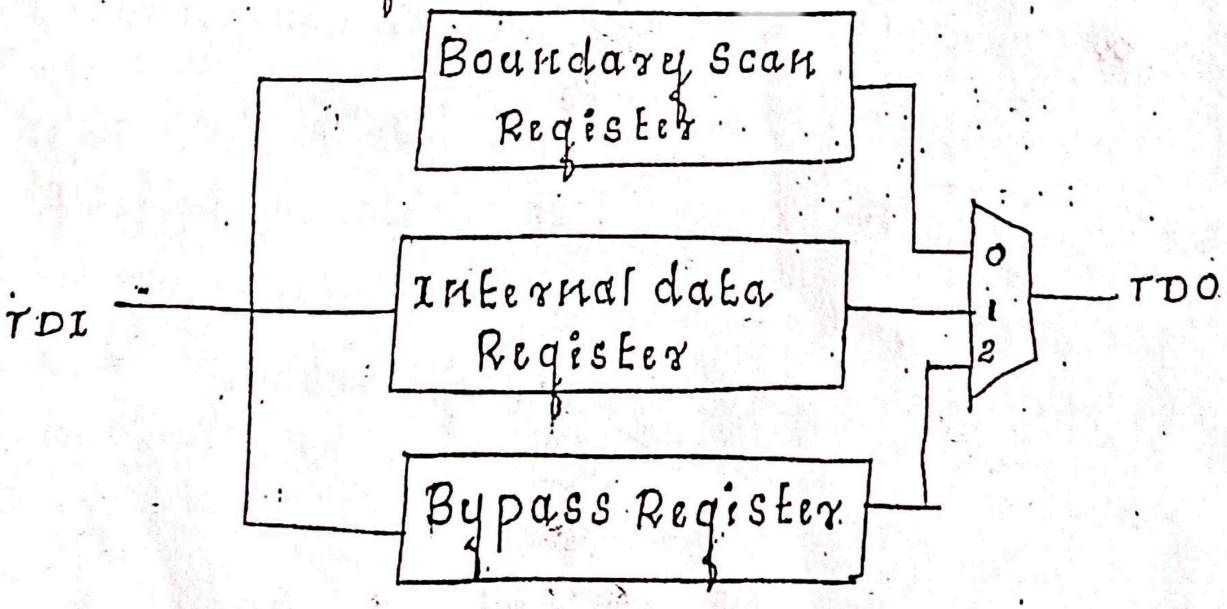
a) Test Access port Interface pins

b) set of test data register → used to collect data from IC

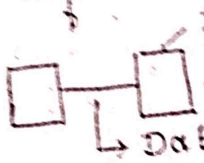
c) Instruction register → used to enable test inputs

d) TAP controller → used to control the flow of data into and out of TAP

TDR (Test data register) Architecture :-



Internal data register:-



* The line going through the I/o pad is data register.

Boundary scan register:-

* It allows the circuit board interconnections to be tested and external components to be tested and state of chip inputs/outputs to be sampled.

Instruction register:-

* It contains atleast 2 bits.

① EXTEST → allows the testing of off chip circuit. In this condition bits of IR sets to one.

② Sample/preload → it allows the IC input/output to be sampled or preloaded.

③ Bypass → it is executed. Then IR bits are made zeros. This instruction bypasses serial data registers in a chip with 1 bit register.

④ Runbist → used to run self testing process steps with in IC.

⑤ Intest → allows single-step testing.

TAP controller:

* Consist of various signals - TCK, TRST, TMS, TDI, TDO, T

PART – A QUESTIONS AND ANSWERS

1. What is the need for testing?

Testing is the process of identifying the fault in the design or IC. The role of testing is detect whether something went wrong in the design.

2. What are the different levels of testing done for a chip?

- At the wafer level
- At the packaged-chip level
- At the system level
- At the board level
- In the field

3. What are the different types of testing?

1. Characterization Testing
2. Production testing
3. burn-in testing
4. Incoming inspection

4. What is characterization testing?

Characterization is the process of debugging the design of new product before it is sent to production. The purpose is to verify:

(i) The correctness of the design

(ii) Whether the device meet all specification

(iii) Verifying the electrical parametric test like AC and DC measurements of the circuit.

5. What is production testing?

After fabrication of IC, the chip is subjected to production tests to ensure the quality requirement by determining whether the device meets specification. It is an outgoing inspection test of each device, and is not repetitive.

6. What is burn-in testing?

Burn-in ensures reliability of tested devices by testing, either continuously or periodically, over a long period of time, and by causing bad devices to actually fail. During burn-in, the IC's are subjected to:

- A combination of production tests.
- Monitoring the IC behavior for high temperature
- Observing the behaviour of the IC for over-voltage power supply.

7. What is incoming inspection test?

System manufacturers perform incoming inspection on the purchased devices before integrating them into the system. The incoming inspection may be done for a random sample with a sample size depending on the device quality and the system requirement.

8. What is functional test?

Functional tests verify the functionality of the device or circuit. Functionality tests verify for a particular input vector whether the device yield the right output or not.

9. What is manufacturing test?

Manufacturing tests are used to verify that every gate operates as expected. The purpose of manufacturing test is to discover any faults caused due to manufacturing defects or errors. Typical errors include:

- Layer-to-layer shorts.
- Discontinuous wires.
- Thin-oxide shorts to substrate or well.

- Nodes shorted to power or ground.
- Nodes shorted to each other.
- Inputs floating/ output disconnected.

10. What is defect?

A defect in an electronic system is the unintended difference between the implemented hardware and its intended design. Some typical defects in VLSI chips are:

- Process Defects - Oxide breakdown, parasitic transistors, missing contact window, etc.
- Age Defects - Electromigration, dielectric breakdown, etc.
- Materials Defects - Crystal imperfection, surface impurities etc.
- Package Defects - Contact degradation, seal leaks etc.

11. What is error?

A wrong output signal produced by a defective system is called an error.

12. What is fault?

A representation of a "defect" at the abstracted function level is called a fault.

13. What is stuck-at fault?

The fault at the interconnection of gates is called stuck-at fault. This fault is modeled by assigning a fixed 0 or 1 value to a signal line in the circuit.

14. What are the two types of stuck-at faults?

1. stuck-at zero (s-a-0)
2. stuck-at one (s-a-1)

15. What is s-a-0 fault?

When logic gate output is always stuck at 0, independent of input values is called stuck-at zero fault.

16. What is s-a-1 fault?

When logic gate output is always stuck at 1, independent of input values is called stuck-at one fault.

17. What is short-circuit fault?

The physical faults like under etching, spiking, diffusion shorts, contact opens, gate oxide imperfections and mask misalignment is called short circuit fault.

18. What is open-circuit fault?

The physical faults like a break in a poly-silicon line, metal migration, stress, peeling and misaligned poor wire bonding is called open-circuit fault.

19. What is controllability and observability?

Controllability for a digital circuit is defined as the difficulty of setting a particular logic signal to a 0 or a 1. Observability for a digital circuit is defined as the difficulty of observing the state of logic signal.

20. What is SCOAP?

Sandia Controllability/Observability Analysis Program. SCOAP consists of six numerical measures for each signal (n) in the circuit.

1. Combinational 0-Controllability, CC0(n)
2. Combinational 1-Controllability, CC1(n)
3. Combinational Observabiltiy,CO(n)
4. Sequential 0-Controllability, SC0(n)
5. Sequential 1-Controllability, SC1(n)
6. sequential observabiltiy, SO(n)

21. What is ATPG?

Automatic Test Pattern Generation is algorithm that injects a fault into a circuit, and then uses a variety of mechanisms to activate the fault and cause its effect to propagate through the hardware and manifest itself at a circuit output. The output signal changes from the value expected for the fault-free circuit, and this causes the fault to be detected.

22. What is D-calculus Algorithm?

The D-calculus algorithm is an ATPG for tracing faults. The symbol D (for detect) indicates the value of a node. The node values are defined by five-valued logic to implement test generation algorithm this consist of the states 1,0,D,$\overline{D}$ and X.

23. What is PODEM algorithm?

The Path – Oriented Decision Making algorithm solves the problem of reconvergent fanout and allows multipath sensitization.

24. What are the classifications of fault simulation?

1. Serial fault simulation
2. Parallel fault simulation
3. Concurrent fault simulation
4. Nondeterministic fault simulation

25. What is delay fault testing?

Delay fault cause the combinational delay of a circuit to exceed the clock period. Specific delay faults are:

What are the advantages of Built-in Self-Test?

- Reduced testing and maintenance cost
- Lower test generation cost
- Reduced storage / maintenance of test patterns
- Simpler and less expensive ATE
- Can test many units in parallel
- Shorter test application times
- Can test at functional system speed

37. What is BILBO?

BILBO – Built-in logic block observer, extra hardware added to flip-flops so that they can be reconfigured as an LFSR pattern generator or response compacter, a scan chain, or as flip flops.

38. What is LFSR?

LFSR – Linear feedback shift register, hardware that generates pseudo-random pattern sequence.

39. What is Pseudo-random testing?

Pseudo-random testing – Algorithmic pattern generator that produces a subset of all possible tests with most of the properties of randomly-generated patterns.

40. What is I_{DDQ} testing?

I_{DDQ} testing is mainly used for bridging faults ie., V_{dd} supply current Quiescent or current supply monitoring.

1. What are the types of faults detected by I_{DDQ} testing?

1. Transistors stuck-open
2. Transistors stuck-closed
3. Transistor gate oxide shorts
4. interconnect bridging shorts
5. unpowered interconnect opens

What is Boundary scan testing?

Boundary scan is a methodology allowing complete controllability and observability of boundary pins of a JTAG compatible device via software control. This capability enables circuit testing without the need of bed-of-nail in-circuit test equipment. Boundary scan vides the following major modes of operation:

- In non-invasive mode
- The pin-permission mode

43. What is TAP?

The Test Assess Port (TAP) controller is a state machine (16 possible states) controlling operations associated with boundary scan cells. The basic operation is controlled through four pins: Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), and Test Data Out (TDO). The TCK and TMS pins direct signals between TAP controller states. The TDI and TDO pins receive the data input and output signals for the scan chain. Optionally, a fifth pin, TRST, can be implemented as an asynchronous reset signal to the TAP controller.

44. What are the different tools available in a typical CAD tool set.

Design rule checker (DRC)
Layout versus Schematic (LVS)
Circuit Extractor
Circuit simulators
Orcad
Simucad
PALASM

45. Define SSI, MSI, LSI and VLSI.

SSI: Small scale Integration where the no of transistor fabricated in an IC is less than 10.

MSI: Medium scale Integration where the no of transistor fabricated in an IC is approximately 10 to 1000 gates.

LSI: Large Scale Integration where the no of transistor fabricated in an IC is thousands of gates.

VLSI: Very large Scale Integration where the no of transistor fabricated in an IC is hundreds of thousands of gates.

46. State all the test vectors to test 3 input NAND gate.

No of test vectors will be $2^3 = 8$

{000, 001, 010, 011, 100, 101, 110, 111}

47. List the design steps required for tesing in CMOS chip design.

Logical verification
Functional verification
Fault testing and coverage
Physical and pre-layout verification
Post layout verification

- Transition faults
- Gate-delay faults
- Line-delay faults
- Segment delay faults
- Path delay faults

26. What is statistical Fault Analysis?

The Statistical Fault Analysis (STAFAN) is another fault – independent technique that statistically determines controllabilities, observabilities, detection probabilities and fault coverage from true value simulation.

27. What is DFT?

Design for Testability (DFT) is set of design rules and guidance for controllability and observability to facilitate the testing of a circuit. Design for testability (DFT) refers to those design techniques that make test generation and test application cost-effective.

28. What are the two methods of DFT?

1. Ad-Hoc
2. Structured methods:
   - Scan
   - Partial Scan
   - Built-in self-test (BIST)
   - Boundary scan

29. What is Ad-Hoc testing?

It is one of the DFT methods for testing the design. The main objectives of Ad-Hoc testing are:

- Avoid *asynchronous* logic feedbacks.
- Make FFs initializable, i.e., provide clear and reset.
- Avoid gates with a large fan-in.
- Provide test control for difficult to control signals.

30. What are the disadvantages of Ad-Hoc testing?

- Experts and tools not always available.
- Test generation is often manual with no guarantee of high fault coverage.
- Design iterations may be necessary.

31. What are the objectives of Scan design method?

- Simple read/write access to all or subset of storage elements in a design.
- Direct control of storage elements to an arbitrary value (0 or 1).
- Direct observation of the state of storage elements and hence the internal state of the circuit.

32. What are scan design rules in testing DFT method?

- Use only clocked D-type flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
- Clocks must not feed data inputs of flip-flops.

33. What is LSSD?

Level Sensitive Scan Design technique, which incorporates two aspects level sensitivity and a scan path approach.

- The level-sensitive aspect means that the sequential network is designed so that when an input change occurs, the response is independent of the component and wiring delays within the network.
- The scan path aspect is due to the use of shift register latches employed as storage element.

34. What are the advantages of LSSD?

1. The circuit operation is independent of the dynamic characteristics of the logic elements rise and fall-times and propagation delays.

2. ATPG is simplified since tests need only be generated for a combinational circuit.

3. LSSD methods, when adopted in design, eliminate hazards and a race greatly simplifies test generation and fault simulation.

35. What is Built-in Self-Test?

Built-in Self-Test are used to determine the correctness of a circuit by examining a signature, which is some statistical property of the circuit.

36. What are the types of testing carry out in Built-in Self-Test?

- Single combinational / sequential stuck-at faults
- Delay faults
- Single stuck-at faults in BIST hardware

48. What is Testers?

A tester is a device which is used to drive the inputs and to monitor the outputs of a device-under-test. Testers are popularly known as ATE [Automatic Test Equipment].

49. What is test fixtures?

A socket for transmitting electrical signals from the test signal generation [IC tester] to an IC device-under-test (DUT) is called test fixtures.

50. What is shmooing?

Shmooing is the ability to vary the voltage and timing on a per-pin basis with a tester. Schmoo plot gives the speed sensitivity of that part with respect to voltage. Schmoo test is the skew timing on the inputs with respect to chip clock to look for setup and hold variation.

51. What is test programs?

A collection of test patterns that has been organized in a certain order and converted to the language (data format) of a specific test platform.

52. What is setup time?

Time the signal must arrive and be stable before the clock edge to ensure capture.

53. Define Input hold time.

Time the signal must remain stable after the clock edge to ensure that capture is stable.

54. Define output valid time.

Time the signal takes to the valid or tristated and stable on the output after the clock edge.

55. Define output hold time.

Time that the signal remains available after output valid so that it can be used.

56. Define handlers.

A device which is responsible for feeding ICs to a test fixture attached to a tester is called IC handler.

57. Define test bench.

A test bench is a virtual environment used to verify the correctness or soundness of a design or model.

58. Define RTL.

Register Transfer Level - a text - based design description where the behavior of a circuit is modeled as dataflow and control from register to register in reference to an applied clock, clocks or other synchronizing signals.

59. What is regression testing?

Testing involves performing a suite of simulations to automatically verify that no functionality has inadvertently changed in a module or set of modules.

60. Define version control.

Version control support to static, dynamic and open configurations, so as to define configurations according to the current development of the design object or to the abstraction level which is desired for a given object presentation. That is orderly management of different design, iterations

61. Define bug tracking.

A bug tracking system is a software application that is designed to help quality assurance and the designer keep track of reported bugs in their work. It may be regarded as a sort of issue tracking system.

61. Define fault model.

A mathematical model of faculty behaviour that can be used to access the compliance of a circuit to various criteria.

62. Define Fault simulation.

The act of simulating a target vector against a good circuit description, and simultaneously a circuit description that contains a fault and comparing both the outputs.

63. What is serial fault simulation?

Simulate two copies of the circuit, the first copy is a good circuit and the second copy of the circuit is inserted with fault. Simulating one faculty circuit at a time and comparing with good circuit.

64. What is parallel fault simulation?

In parallel fault simulation m words in an n-bit computer are used to encode the state of n circuits for a 2^m - state simulator.

65. What is concurrent fault simulation?

Concurrent fault simulation uses a non faulted version of the circuit to create a good machine model. Each fault creates a new faculty machine that is simulated in parallel with the good machine. Thus $N+1$ simulations may have to be completed, where N is the number of faults.

66. What is Nondeterministic fault simulation?

Simulate a subset or sample of the faults and extrapolate fault coverage from the sample.

67. Define fault sampling.

It is the ratio of detected fault to all faults in the sample is used as an estimate of the fault coverage in the complete fault set.

68. Define Fault coverage.

The metric of how many faults are exercised and successfully detected (their fault effect is observed) versus the total number of faults in the circuit-under-test.

69. Define yield.

Yield is defined as the function (or percentage) of acceptable parts among all fabricated parts.

70. What is ATE?

The Automatic Test Equipment is an instrument used to apply test patterns to a device-under-test, analyze the responses from the DUT, and mark the DUT as good or bad.

71. What are the initial set-up procedure for a tester to run test programs?

- Set the supply voltages.
- Assign mapping between stimulus file, signal names and physical tester pin.
- Set the pins on the tester to be inputs or outputs and their V_{OH}/V_{IH} levels.
- Set the clock on the tester.
- Set the input pattern and output assertion timing.

72. Define test vectors.

The binary input bit patterns are called test vectors which is used to verify the functionality of the device-under-test.

73. What are the different format of test data?

1. Non-Return-to-zero (NRZ)
2. Return-to-zero (RZ)
3. Surrounding-by-complement (SBC)

74. What are the tests that are verified using regression testing?

Regression testing attempts to verify

- That the application works as specified even after the changes / additions / modifications were made to it.
- The original functionality continues to work as specified even after changes / additions / modifications to the design application.
- The changes / additions / modifications to the design have not introduced new bugs

Part-A

1. What is the aim of adhoc test techniques (Nov 2007)
2. Distinguish functionality test and manufacturing test (Nov 2007).
3. State the need for testing. (April 2008)
4. List the design steps required for testing in CMOS chip design. (April 2008)
5. What are the different types of CMOS testing (Nov 2008)
6. What is IDDQ testing (April 2010)
7. Define Controllability and Observability (Nov 2010)
8. What are the test fixtures required to test chip (Nov 2011)
9. What are the advantage of a single stuck at fault (May 2012)
10. List the basic types of CMOS testing (May 2013)

Part-B

1. Explain in detail Boundary Scan test. (April 2008)
2. Explain with diagram the design strategies for testing the CMOS devices (Nov 2008)
3. Discuss the issues in design for testability (Nov 2010)
4. Discuss in detail the various testing approaches that are used to determine the defects during manufacturing. (May 2011)
5. Describe the adhoc testing and scan based approaches to design for testability (Nov 2011)

6. Explain the principle of silicon debug (May 2012) (May 2013)

Chapter 8 Verification and Testing

- Objectives
  - Fault modeling and simulation
  - Test generation
  - Automatic-test-pattern-generation
  - Built-in-self-test
  - BIST architecture
  - Scan and boundary scan
  - Scan chains
  - Digital scan standard

Introduction

- Digital system verification and testing are progressively more important, as they become major contributors to the manufacturing cost of a new IC product.
- The emphasis on the quality of the shipped products, in addition to the growing complexity of VLSI design, requires testing issues to be considered early in the design process so that the design can be adjusted to simplify testing procedures.

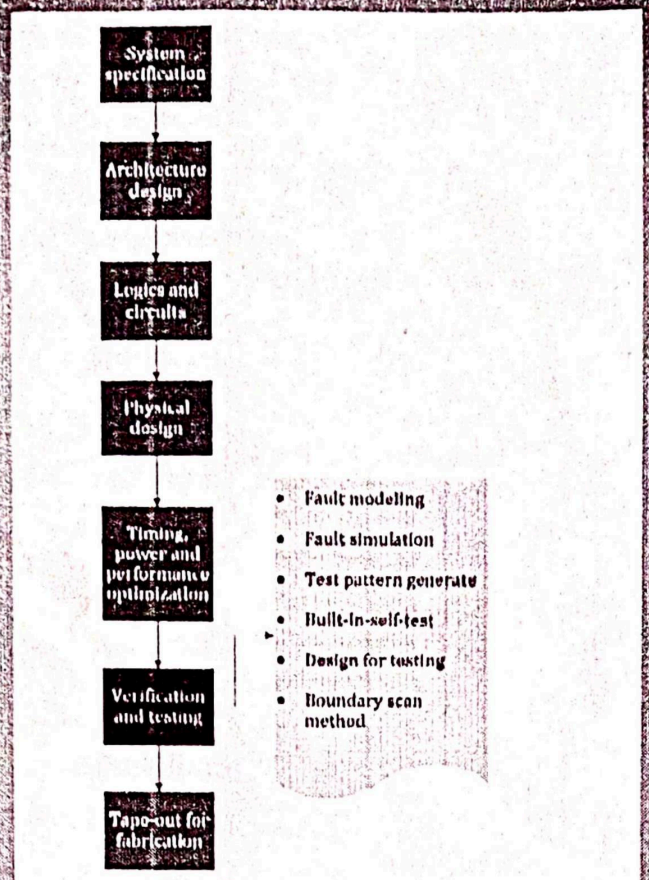


Figure 8-1 Verification and testing in the design flow

- Figure 8-2 demonstrates a VLSI development process in hierarchies.

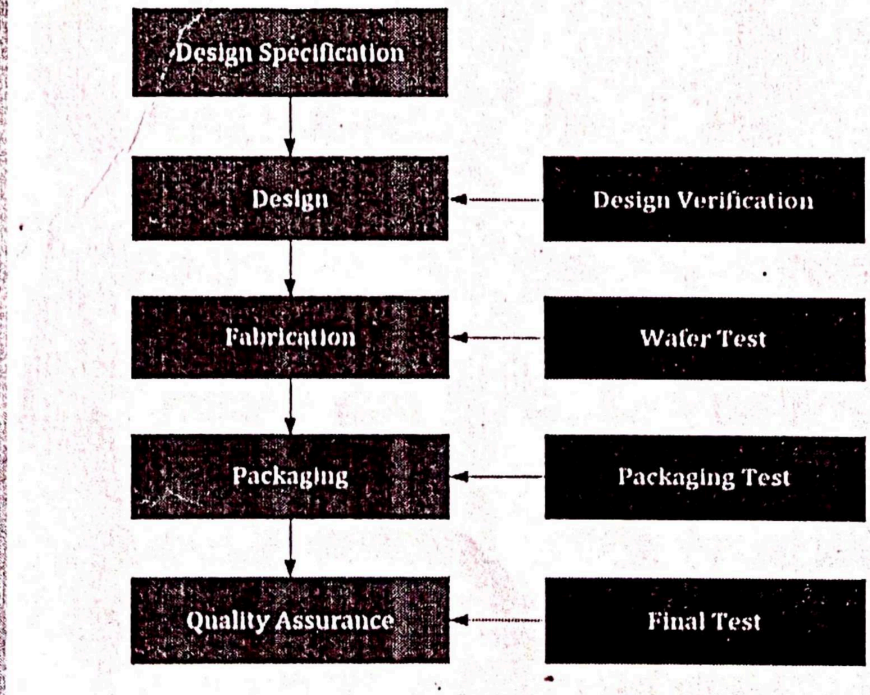


Figure 8-2 VLSI development process (Wang, Wu, & Wen, 2006)

- Based on customer or project need, a VLSI device requirement is determined and formulated as a design specification.
- Then, the designers synthesize a circuit that satisfies the design specification and verify the design.
- Design verification is a predictive analysis that ensures the synthesized design will perform the required functions when manufactured.
- When a design error is found, modifications to the design are necessary and design verification must be repeated.

- Once verification is done, the VLSI design is ready to be fabricated.
- At the same time, test engineers develop a test procedure based on the design specification and fault models associated with the implementation technology.
- Then, the chips that pass the wafer-level test are extracted and packaged.
- The packaged devices are retested to eliminate those devices that may have been damaged during the packaging process or put into defective packages.
- Additional Quality Assurance testing is used to assure the final quality before going to market.

- A typical circuit testing process is illustrated in Figure 8-3, which consists of applying a set of test stimuli to the inputs of the circuit under test (*CUT*) while analyzing the output responses.

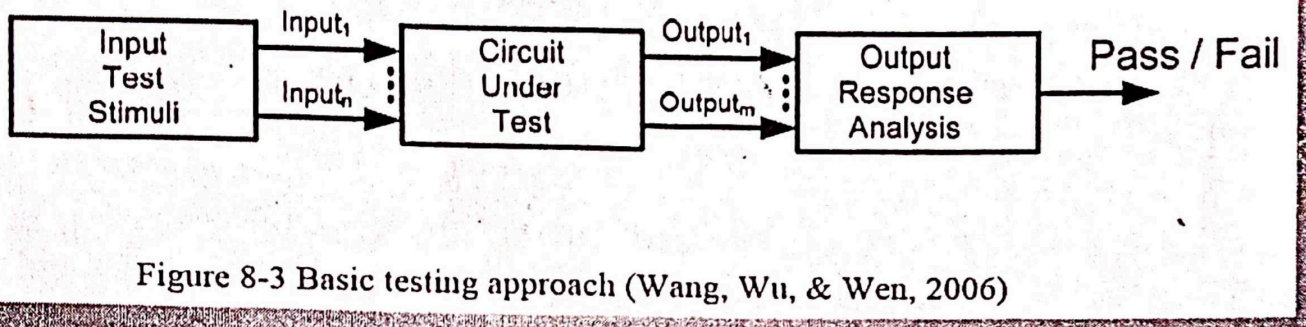


Figure 8-3 Basic testing approach (Wang, Wu, & Wen, 2006)

Fault Model

- Because of the diversity of VLSI defects, it is difficult to generate tests for real defects.
- Fault models are necessary for generating and evaluating a set of test vectors.
- There are many types of fault models, like "open and short fault", "bridging fault", "delay fault", "coupling fault", and so on.
- Generally, a good fault model should satisfy two criteria:
  - It should accurately reflect the behavior of the defects.
  - It should be computationally efficient in terms of fault simulation and test pattern generation.

- Because of the diversity of VLSI defects, it is difficult to generate testing patterns for real defects.
  - Fault models are necessary for generating and evaluating a set of test vectors.
- Good fault models can abstract physical defects in the circuit at a high level and represent a high percentage of the actual physical defects that can occur in components.
  - They allow test generation and fault/coverage analysis to be done early in the design process.
- A combination of different fault models is often used in the generation and evaluation of test vectors and testing approaches developed for VLSI devices.

- An example

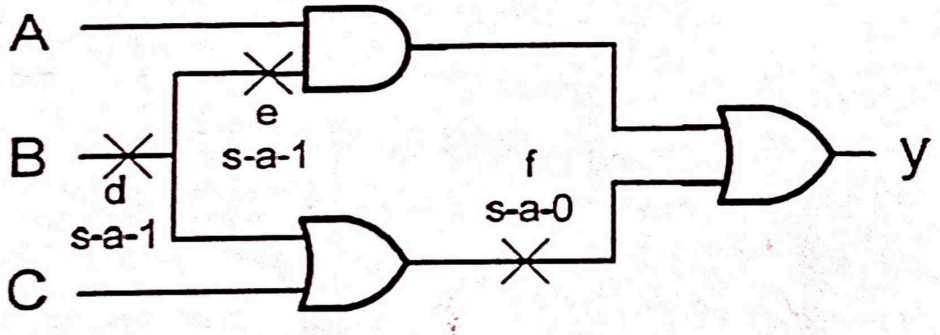


Figure 8-5 An example of a single stuck-at fault.

- How to find the fault
  - Testing vector

Consider the circuit in Figure 8-5. Three stuck-at faults (*d*, *e*, and *f*) are marked in the circuit. It is apparent that the fault-free function of output $y = (AB) + (B + C)$. The faulty functions are (note: the fault *d s-a-1* can also be written as "*d SA1*", or "*d/1*" for short):

d/1 fault: $y = (A \cdot 1) + (1 + C) = A + 1 = 1$

e/1 fault: $y = (A \cdot 1) + (B + C) = A + B + C$

f/0 fault: $y = AB + 0 = AB$

- Fault analysis procedure
  - The stuck-at fault model, which has been successfully and most commonly used for decades, is a logical and easy-to-understand fault model.
  - The process of a stuck-at fault model testing is shown in Figure 8-4.

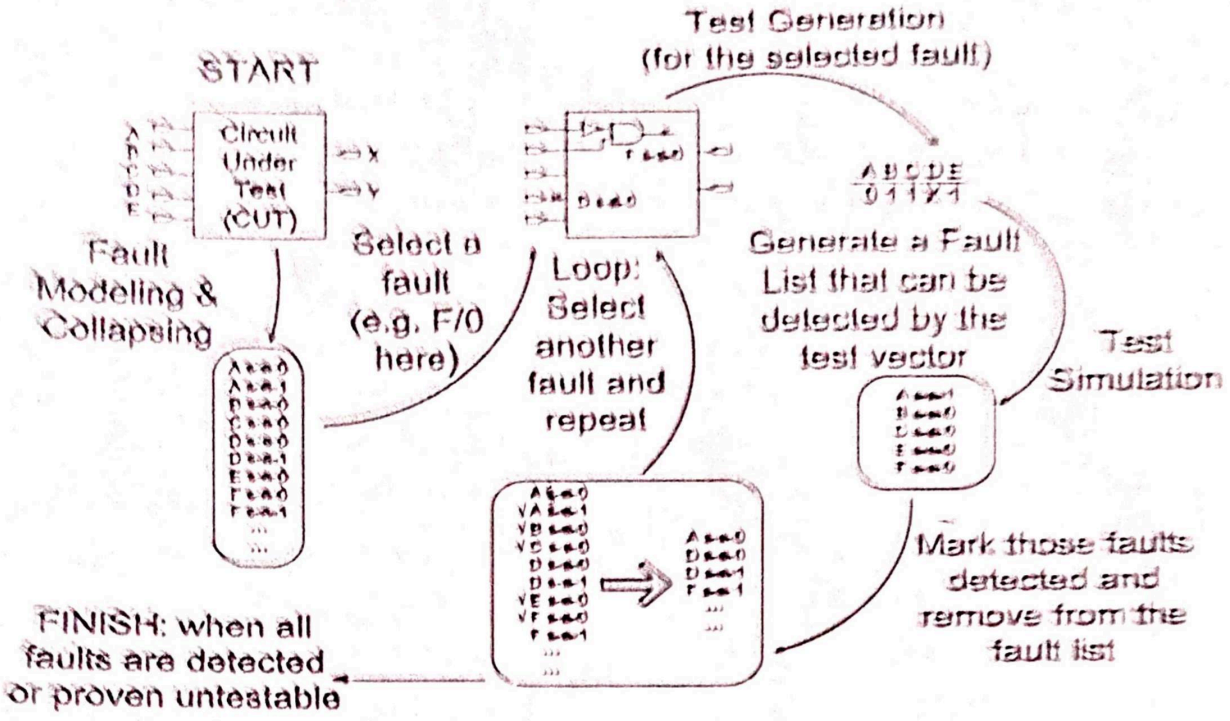


Figure 8-4 Fault analysis procedure

Fault Simulation

- Logic simulation for a combinational logic circuit is the determination of steady-state logic values implied at each circuit line by the vector applied to its primary inputs.
- A high-quality fault simulation to predict the faulty circuit behavior can greatly improve testing and diagnosis.
- The purpose of fault simulation is to evaluate the effectiveness of a set of test patterns in detecting manufacturing defects.
- The quality of a test set is expressed in terms of fault coverage, the percentage of faults that causes an incorrect output if the test set is applied.
- Furthermore, it helps identify undetected faults. In this case, the test designer has to generate additional test vectors to improve the fault coverage.

Automatic-Test-Pattern-Generation

- Automatic test equipment (ATE) is computer-controlled equipment used in the production testing of ICs (both at the wafer level and in packaged devices) and PCBs.
- Test patterns are applied to the CUT and the output responses are compared to stored responses for the fault-free circuit.
- Generating effective test patterns efficiently for a digital circuit is thus the goal of any Automatic-Test-Pattern-Generation (ATPG) system.
- A powerful ATPG can be regarded as the Holy Grail in testing, with which all Design-for-testability (DFT) methods could potentially be eliminated.

Built-In-Self-Test (BIST)

- As mentioned before, testing ought to be quick and have very high fault coverage. One approach is to inset a testing circuit as one of the system functions, so it becomes capable of self-test.
- Built-In-Self-Test (BIST) refers to techniques and circuit configurations that enable a chip to test itself.
- BIST techniques can be classified into two categories, online-BIST and offline-BIST.
  - Online-BIST includes concurrent and nonconcurrent BIST, whereas offline-BIST consists of functional and structural approaches.

The Concept of BIST

- Traditional test techniques using ATPG software to target single faults for digital circuit testing have become quite expensive and can no longer provide adequately high fault coverage for deep submicron or nanometer designs.
- One practical approach to solve these testing problems is to incorporate BIST features into a digital circuit.
- Logic BIST is a design for testability (DFT) technique in which a portion of a circuit on a chip, board, or system is used to test the digital logic circuit itself.
  - In this methodology, test patterns are generated on-chip and test responses are also analyzed on-chip. The basic of BIST designs has a Test pattern generator (TPG) and an output response analyzer (ORA) as shown in Figure 8-23.

- BIST system structure

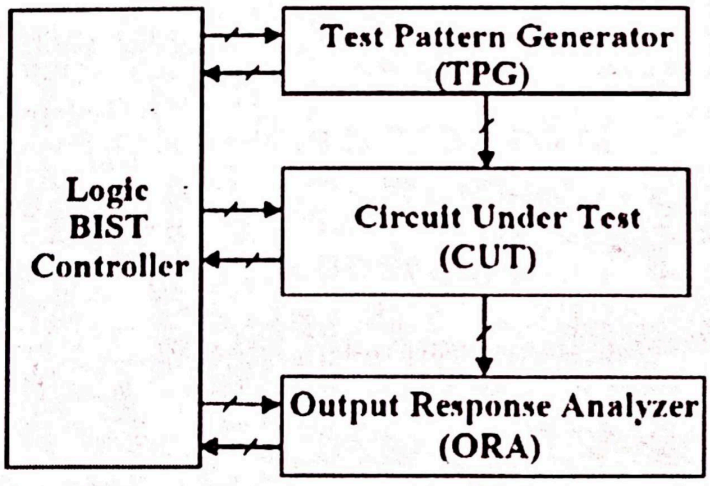


Figure 8-23 A structural offline-BIST system

- BIST offers several advantages over testing using automatic test equipment (ATE).
  - First, in BIST the test circuit is integrated on-chip so that no external tester is required.
  - Second, a self-testable chip enables self-test to execute even after it is built into a system. This can be used either for periodic testing or to diagnose system failures.
  - Third, self-test can be performed at the circuit's normal clock rate, since it's getting more and more difficult for ATE to keep pace with the increasing circuit speeds.

- Figure 8-24 gives a typical BIST hardware in more detail.
  - A comparator compares the signature produced by the data compacter with a reference signature stored in a ROM during BIST.

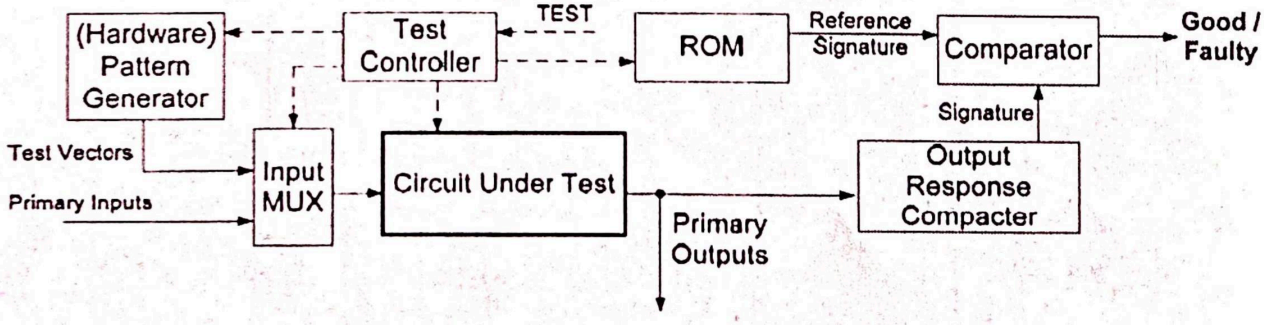


Figure 8-24 BIST Process

Scan and Boundary Scan

- Testability is a design feature which influences the cost of testing.
- Two important attributes, controllability and observability, are highly associated with testability.
  - Controllability for a digital circuit is the difficulty of setting a particular logic signal to '0' or '1'.
  - Observability is the challenge of observing the state of a logic signal at a particular point in the circuit.

- Those circuits have difficulty to control are decoders, circuits with feedback, oscillators, and so on; whereas low observability circuits are sequential circuits, embedded RAM, ROM or PLAs, etc.
- Control logic, random logic, and asynchronous design are more difficult to test than the combinational logic, data-path logic, and synchronous design.

- The main idea in scan DFT design is to obtain controllability and observability for flip-flops.
  - This is done by adding a test mode to the circuit, in addition to its normal mode. In the normal mode, the flip-flops are connected as shown in Figure 8-46.
  - During this mode, the response at the state outputs (Y_1 to Y_k) is captured in the flip-flops. These values can be observed by switching the circuit to test mode, whose flip-flops are reconfigured as one or more shift-registers, called scan registers or scan chains.
  - In addition, values to be applied at the state inputs in the subsequent test may be simultaneously shifted into the flip-flops.
  - Thus, for the purposes of test development, the state inputs and outputs can be treated as being similar to primary inputs and outputs, respectively.

- Normal sequential logic structure

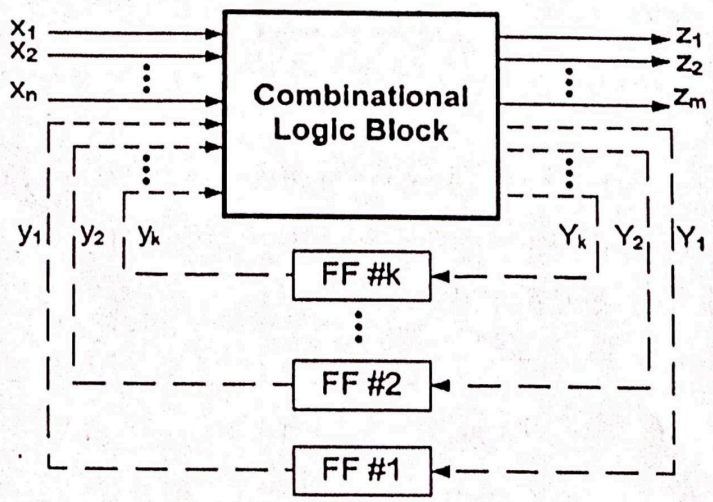
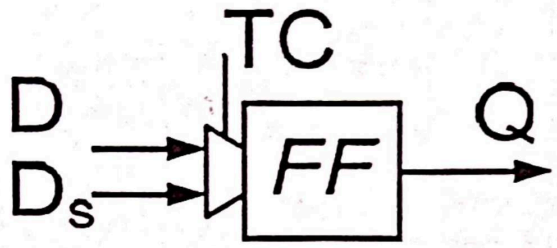


Figure 8-46 A special view at a general model of a sequential circuit (Jha & Gupta, 2003)

- Replace the normal flip-flop by scan flip-flop



(a) A view of scan flip-flop

- A sequential logic with scan flip-flop

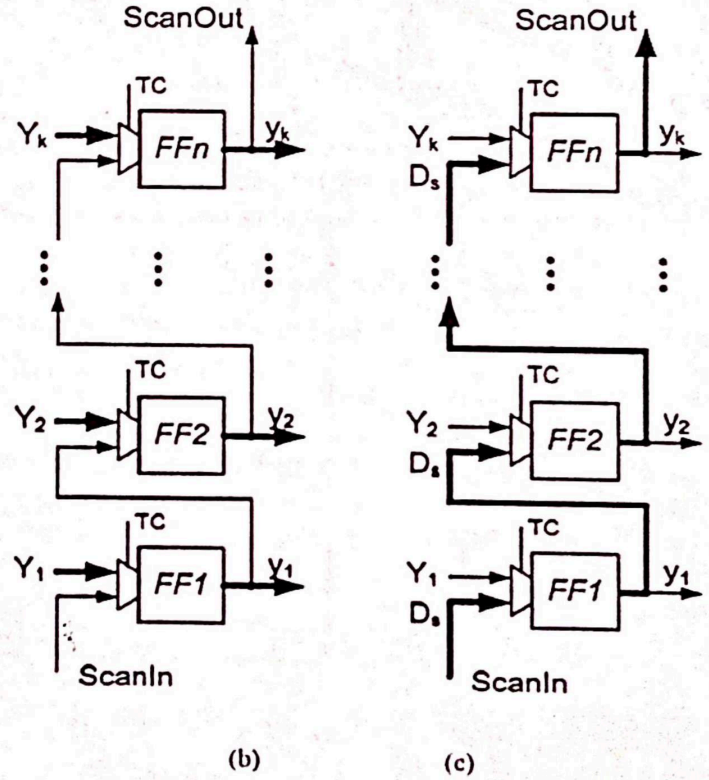


Figure 8-47 (a) A view of scan flip-flop. (b) a scan structure working under normal mode and (c) a scan structure working under test mode

- General logic structure with "scan capability"

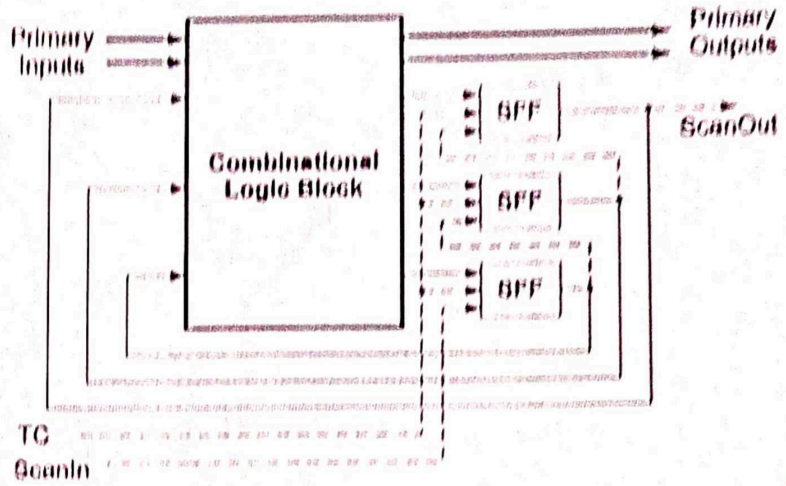


Figure 8-48 The complete block diagram of scan DFT design (Bushnell & Agrawal, 2002)

- Operation of the circuit with scan flip-flop

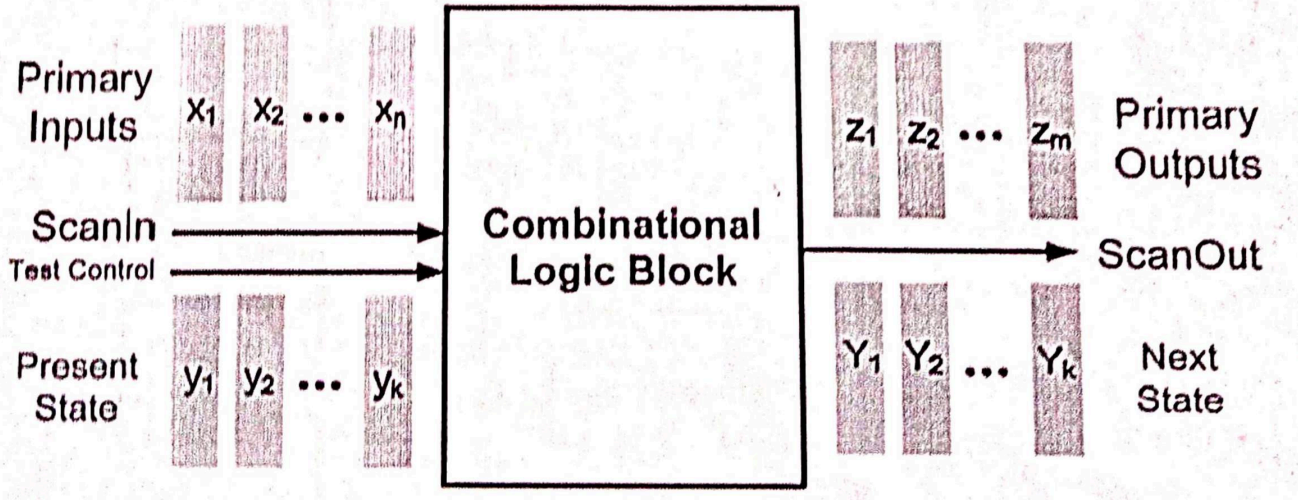


Figure 8-49 Combinational test vectors (x_i, y_i, z_i, and Y_i have the same meaning as it in Figure 8-46)

Scan Chains

- Scan testing is very useful, but it brings higher costs, which can be categorized into two types.
- First, the scan hardware increases the chip size (area overhead) and second, it slows the signals down (performance overhead).
- Area overhead is typically found to be 5% to 10%, because of using "scan flip-flops" and wiring them.
- Adding multiplexer delay into the combinational path results in approximately two gate-delays, and flip-flop output loading due to one additional fanout produces approximately 5% to 6%.
- Overall, scan design can cause a 5 to 10% reduction in speed.

- To overcome the above shortcomings, scan flip-flops can be organized into chains by using Partial Scan, partitioning them into multiple chains, ordering flip-flops within each chain, and using a reconfiguration circuit.
- For ease of representation, combinational circuit elements are combined into a number of combinational blocks using the following procedure.
  - First, each combinational circuit element is treated as an individual block. If any element in one block is hooked up via a combinational connection to any element in another block, then these two are combined into a single block.
  - This process is repeated until no two blocks can be combined, *i.e.*, blocks of maximal size are obtained. Let CLB_1, CLB_2, …, CLB_N be the Combinational Logic Blocks obtained in this methodology. Subsequently, the flip-flops may be combined into multi-bit parallel-load registers (Jha & Gupta, 2003).

- An example

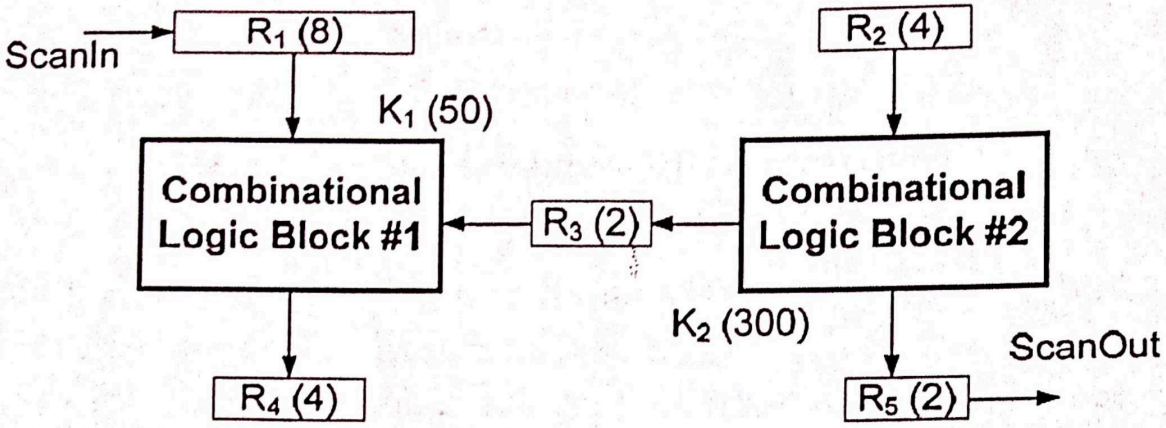


Figure 8-51 An example circuit with two CLBs and five registers configured as a single chain (Jha & Gupta, 2003)

- An outline of a typical test procedure using a boundary scan is as follows:
  - A boundary-scan test instruction is shifted into the IR through the TDI.
  - The instruction is decoded by the decoder associated with the IR to generate the required control signals so as to properly configure the test logic.
  - A test pattern is shifted into the selected data register through the TDI and then applied to the logic to be tested.
  - The test response is captured into some data register.
  - The captured response is shifted out through the TDO for observation and, at the same time, a new test pattern can be scanned in through the TDI.
  - Steps 3 to 5 are repeated until all test patterns are shifted in and applied, and all test responses are shifted out.

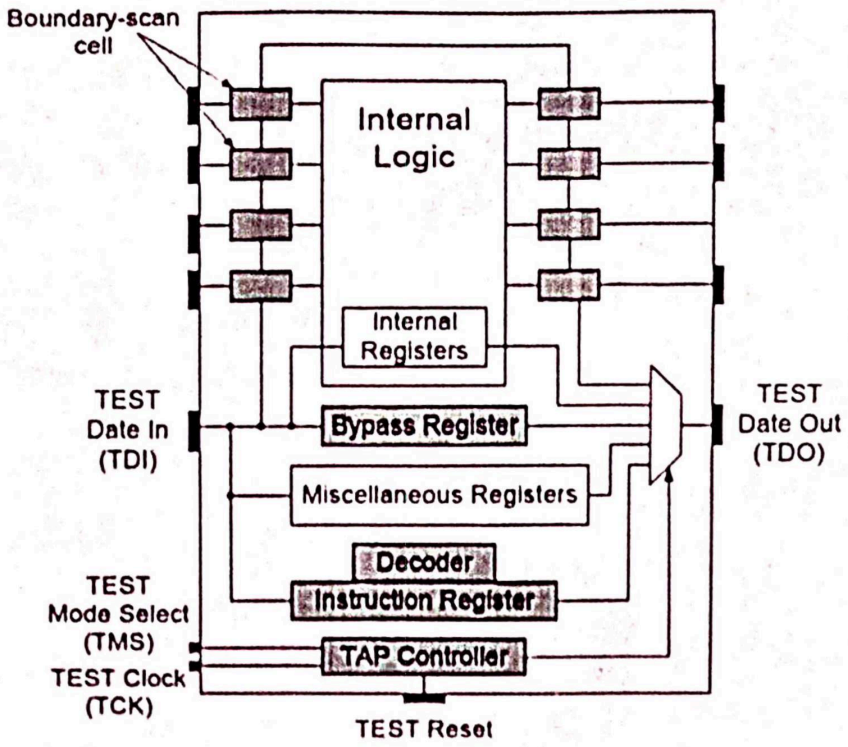


Figure 8-57 Boundary-scan architecture
Note: The four terminals— test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK) — are mandatory terminals of TAP.

Summary

- In this section we have discussed the verification and testing.
- Each of these two subjects itself is a deep and broad area in VLSI design.
  - What has been discussed in this chapter is only introductory material, but is self-contained.
- Today, most testing circuits and testing vectors are generated automatically by CAD tools.
- It is necessary for a designer to understand what circuit has been inserted into the chip for testing and how it works.
- Readers can try to design and insert the testing circuit in the project MSDAP.